Lecture 15
Multistage FET Amplifiers

In this lecture you will learn:

• Multistage FET Amplifiers
• The Cascade Design
• The Cascode Design

The Need for Multistage Amplifiers

Most modern amplifiers have multiple stages in order to:

1) Increase the amplifier gain (voltage gain or current gain or transimpedance gain or transconductance gain)

2) Transform the input resistance to match the source

3) Transform the output resistance to match the load
A Cascade of Two CS Stages for a Voltage Amplifier

![Circuit Diagram]

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in

R

0

+  

-  

2

in

v

A

2

in

v

A

2

out

+  

-  

out
A Cascade of Two CS Stages: Finding Input Resistances

1) First find $R_{\text{in}2}$ (input resistance of the last stage):

Make sure $R_L$ is in place!!

$$R_{\text{in}2} = \infty$$


2) Then find $R_{\text{in}1}$ (input resistance of the second last stage):

Make sure $R_{\text{in}2}$ is in place!!

$$R_{\text{in}1} = \infty$$


A Cascade of Two CS Stages: Finding Output Resistances

1) First find $R_{\text{out}1}$ (output resistance of the first stage):

Make sure $R_S$ is in place!!

$$R_{\text{out}1} = (r_{o1} \parallel r_{oc1})$$


2) Then find $R_{\text{out}2}$ (output resistance of the second stage):

Make sure $R_{\text{out}1}$ is in place!!

$$R_{\text{out}2} = (r_{o2} \parallel r_{oc2})$$
A Cascade of Two CS Stages: Finding Voltage Gains

1) Open circuit voltage gains of CS stages do not depend on how the stages are connected (i.e. on source or load resistances)

Stage 1 Parameters:
\[ R_{in1} = \infty \]
\[ R_{out1} = (r_{o1} \parallel r_{oc1}) \]
\[ A_{v1} = -g_{m1}(r_{o1} \parallel r_{oc1}) \]

Stage 2 Parameters:
\[ R_{in2} = \infty \]
\[ R_{out2} = (r_{o2} \parallel r_{oc2}) \]
\[ A_{v2} = -g_{m2}(r_{o2} \parallel r_{oc2}) \]

A Cascade of Two Amplifiers

The two stages can be combined into a single stage:

Input resistance:
\[ R_{in} = R_{in1} \]

Output resistance:
\[ R_{out} = R_{out2} \]

Open circuit voltage gain:
\[ A_v = ? \]
A Cascade of Two Amplifiers

The two stages can be combined into a single stage:

Open circuit voltage gain:

\[ v_{out} = A_v v_{in} = A_v A_{v1} v_{in1} \frac{R_{in2}}{R_{out1} + R_{in2}} \]

\[ A_v = A_v A_{v1} \frac{R_{in2}}{R_{out1} + R_{in2}} \]

Inter-stage voltage divider

A Cascade of Two Amplifiers with a Source Resistor

Voltage gain:

\[ v_{out} = A_v v_{in} \frac{R_L}{R_{out2} + R_L} = A_v A_{v1} v_{in1} \frac{R_{in2}}{R_{out1} + R_{in2}} \frac{R_L}{R_{out2} + R_L} \]

\[ = A_v A_{v1} v_{in1} \frac{R_{in2}}{R_{out1} + R_{in2}} \frac{R_L}{R_{out2} + R_L} \]

\[ = A_v A_{v1} v_{s} \frac{R_{in1}}{R_s + R_{in1}} \frac{R_{in2}}{R_{out1} + R_{in2}} \frac{R_L}{R_{out2} + R_L} \]

\[ \Rightarrow v_{out} = A_v A_{v1} \frac{R_{in1}}{R_s + R_{in1}} \frac{R_{in2}}{R_{out1} + R_{in2}} \frac{R_L}{R_{out2} + R_L} \]

Input voltage divider  Inter-stage voltage divider  Output voltage divider

For the CS FET stages:

\[ R_{in1} = R_{in2} = \infty \]
A Cascade of Two Amplifiers with a Source Resistor

**Voltage gain:**

\[
V_{out} = A_v V_{in} \frac{R_L}{R_{out} + R_L}
\]

\[
= A_v V_s \frac{R_{in}}{R_s + R_{in}} \frac{R_L}{R_{out} + R_L}
\]

\[
\Rightarrow \frac{V_{out}}{V_s} = A_v \frac{R_{in}}{R_s + R_{in}} \frac{R_L}{R_{out} + R_L}
\]

Input voltage divider Output voltage divider

It is easier to use the single-stage model

The expression is the same as the one on the previous slide

A Cascade of Two CS Stages for a Voltage Amplifier

**Putting it all together:**

**Input resistance:**

\[R_{in} = \infty\]

**Output resistance:**

\[R_{out} = r_{o2} \parallel r_{oc2}\]

**Open circuit voltage gain:**

\[A_v = \frac{V_{out}}{V_{in}} = A_{v1} A_{v2}\]

\[= [-g_{m1} (r_{o1} \parallel r_{oc1})] [-g_{m2} (r_{o2} \parallel r_{oc2})]\]

Not really a good voltage amplifier – output resistance is too large – but a decent transconductance amplifier
A Cascade of Three FET Stages: 2 CS and 1 CD

Input resistance:
\[ R_{\text{in}} = \infty \]

Output resistance:
\[ \frac{1}{R_{\text{out}}} \approx \frac{1}{r_{\text{oC}3}} + (g_{m3} + g_{mb3}) \approx (g_{m3} + g_{mb3}) \]

Open circuit voltage gain:
\[ A_v = A_{v1}A_{v2}A_{v3} \]

\[ \approx [-g_{m1}(r_{o1} \parallel r_{oC1})][-g_{m2}(r_{o2} \parallel r_{oC2})][-1] \]

Small

Now it is a better voltage amplifier!

In a direct-coupled scheme, as above, the DC bias of one stage affects the DC bias of other stages.

Need to ensure appropriate DC bias of every stage such that:

i) The FETs are operating in saturation
ii) The desired voltage swing does not cause problems (e.g. cause some FET to go out of saturation)
A Cascade of Three FET Stages: A Better DC Biasing

The sizes (W/L ratios) of M4, M5, and M6 can be adjusted to get the desired bias currents for the three amplifier stages.

A Cascade of CS and CG: A Capacitively-Coupled Cascode

The FET cascode has a large input resistance, a very large output resistance, and a large gain.

But it is much better than a CS-CS cascade in terms of the frequency performance, as we will see later in the course.

The above topology can be simplified........
A Cascade of CS and CG: A Direct-Coupled Cascode

One current source can bias both the stages in a direct-coupling topology....!
This is the preferred way for on-chip designs.

A Cascade of CS and CG: The Cascode

A different way to draw the same circuit.
The FET Cascode: Input and Output Resistances of Each Stage

**Input resistances:**
\[
R_{in2} \approx \frac{1}{g_{m2} + g_{mb2}} \left( 1 + \frac{r_{oc}}{r_{o2}} \right)
\]
Assuming \( r_c = \infty \)
\[
R_{in1} = \infty
\]
\[
\Rightarrow R_{in} = R_{in1} = \infty
\]

**Output resistances:**
\[
R_{out1} = r_{o1}
\]
\[
R_{out2} = r_{oc} \parallel \left[ r_{o2} + R_{out1} + r_{o2} (g_{m2} + g_{mb2}) R_{out1} \right]
\]
\[
\approx r_{oc} \parallel \left[ (g_{m2} + g_{mb2}) r_{o1} r_{o2} \right]
\]
\[
\Rightarrow R_{out} = R_{out2} = r_{oc} \parallel \left[ (g_{m2} + g_{mb2}) r_{o1} r_{o2} \right]
\]

The FET Cascode: Voltage Gains of Each Stage

**Voltage Gains:**
\[
A_{v1} = -g_{m1} r_{o1}
\]
\[
A_{v2} = \left( g_{m2} + g_{mb2} \right) \left( r_{o2} \parallel r_{oc} \right)
\]
\[
A_v = \frac{v_{out}}{v_{in}} = A_{v2} A_{v1} \left( \frac{R_{in2}}{R_{out1} + R_{in2}} \right) = \left( -g_{m1} r_{o1} \right) \left( g_{m2} + g_{mb2} \right) \left( r_{o2} r_{oc} \right) \frac{r_{o2} + r_{oc}}{(g_{m2} + g_{mb2}) r_{o1} r_{o2} + r_{oc}} + 1
\]

If \( r_{oc} \gg r_{o2}, r_{o1} \):
\[
A_v = \left[ -g_{m1} r_{o1} \right] \left( g_{m2} + g_{mb2} \right) r_{o2} \gg \text{Very large}
\]
The FET Cascode: Voltage Gains of Each Stage

Voltage Gains:

\[ A_{v1} = -g_m r_{o1} \quad \text{and} \quad A_{v2} = \left( g_{m2} + g_{mb2} \right) \left( r_{o2} || r_{oc} \right) \]

\[ \Rightarrow A_v = \frac{v_{out}}{v_{in}} = A_{v2} A_{v1} \frac{R_{out2}}{R_{out1} + R_{in2}} = \left( -g_m r_{o1} \right) \left( g_{m2} + g_{mb2} \right) \frac{r_{o2} r_{oc}}{r_{o2} + r_{oc}} \left( g_{m2} + g_{mb2} \right) \frac{r_{o1}}{r_{o1} + r_{oc}} + 1 \]

If \( r_{oc} \sim r_{o2}, r_{o1} : \)

\[ \Rightarrow A_v = \left( -g_m r_{o1} \right) \left( g_{m2} + g_{mb2} \right) \frac{r_{o2} r_{oc}}{r_{o2} + r_{oc}} \left( g_{m2} + g_{mb2} \right) \frac{r_{o1}}{r_{o1} + r_{oc}} \]

\[ \Rightarrow A_v = -g_m r_{oc} \quad \text{can still be large} \]

The FET Cascode: Transconductance Gain

Transconductance Gain (with output shorted):

\[ G_m = \frac{i_{out}}{v_{in}} = \frac{A_v}{R_{out}} \approx -g_{m1} \]
Choose voltage biasing such that:

\[ I_{D1} = I_{D2} = I_{BIAS} \]

Need to realize this voltage source

Use a PFET to implement the current source

Problem: To be accurate with voltage biasing, one needs to know the characteristics (i.e. \( k_n \), \( k_p \), etc) of the FETs accurately, and this information is usually not available to the circuit designer.

Solution: Use circuit biasing schemes that are not too sensitive to the circuit designer's detailed knowledge of the FETs!
Biasing the FET Cascode Amplifier

Choose voltage biasing such that:
\[ I_{D1} = I_{D2} = -I_{D3} = \ldots \]
\[ = -I_{D4} = I_{BIAS} \]

Need to realize this voltage source

What if we have only a single stable current source available on the chip..?
Biasing the FET Cascode Amplifier

Current mirror

M4 and M3 are matched

M5 and M2 are matched

M6 and M1 are matched

Resistance looking into a voltage source must be small

Current mirror

M4 and M3 are matched

PFET current source (does not have large enough $r_{oc}$)
Improved FET Cascode Amplifier

Current mirror

M9 and M8 are matched
M4 and M3 are matched

FET voltage source

M5 and M2 are matched

Cascode PFET current source

M9 and M8 are matched
M4 and M3 are matched