A Model Study of Multilevel Signaling for High-Speed Chiplet-to-Chiplet Communication in 2.5D Integration

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2020 IFIP/IEEE 28th International Conference on Very Large Scale Integration (VLSI-SOC) | 978-1-7281-5409-1/20/$31.00 ©2020 IEEE | DOI: 10.1109/VLSI-SOC46417.2020.9344081

***Abstract*— The quest for high yield has motivated significant advancement in 2.5D integrated circuits, where chiplets are integrated on a silicon interposer or a package substrate with high-speed parallel communication among them. These channels for 2.5D integrated systems need to have high data bandwidth per unit length (also called shoreline-BW-density and measured in Gb/s/mm) and lower energy per bit area (measured in pJ/b). Typically, NRZ signalling is used but achieving higher data rates continues to be a major challenge. In this paper we explore PAM4 as an alternative to NRZ for signalling the channels. Simulations show that we can achieve up to 63% more energy-efficiency and 27% higher BW density for 2.5D integrated systems.**

Keywords*— *Heterogeneous Integration, Coplanar Microstrip, NRZ, PAM4, Channel Operating Margin

I. INTRODUCTION

Heterogeneous 2.5D integration is one of the promising technologies that can increase system yield as well as alleviate the memory bandwidth bottlenecks for microprocessors. Several 2.5D and 3D chip stacking technologies have been recently demonstrated by both the foundries as well as academic groups, including silicon interposers, Embedded Multi-Interconnect Bridge (EMIB), Foveros, CoWoS, HIST. These technologies continue to evolve and address the challenges associated with the slowing down of Moore's Law.

The number of chiplet to chiplet interconnects per unit area that can be achieved, depends on the technology which governs the interconnect pitch. From a signalling perspective, as the pitch decreases, more of the interconnects (also known as physical IO) get packed in much smaller area leading to higher shoreline-BW-density albeit with increased crosstalk and interference. In this article, we explore the design space of fine-pitch interconnects and evaluate multiple signalling schemes for their applicability in 2.5D systems.

In this paper we first model the channel that characterizes the chiplet to chiplet connections in such integrated systems. One such prototypical system is shown in Fig. 1. We introduce the scattering parameters of the channel for different pitches and channel lengths and systematically study two signalling schemes. The highest frequency of operation for each pitch/length configuration is determined. Further, simple transceiver models are used to estimate the energy-efficiency of transmission to quantify energy/bit. The rest of the paper is

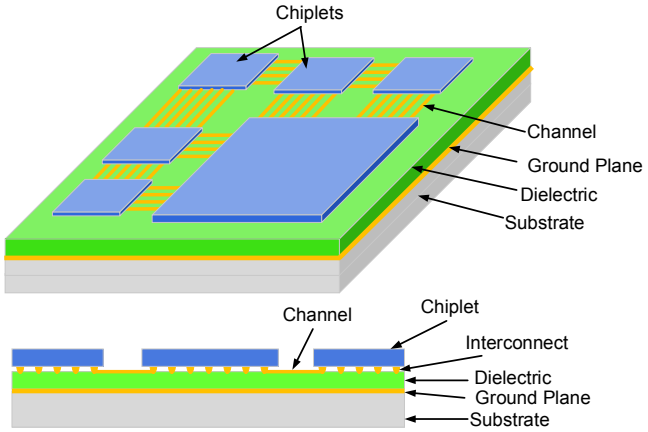

Fig. 1. General model of Heterogeneous Integrated System

organized as follows. Section II briefs the previous works and current state of art for the integration technology. Section III describes the channel model. Section IV elaborates on the transceiver system with its different components. In section V, the channel simulation setup is explained along with the methods and metrics for simulation. Section VI describes the power estimation and explores the entire design space. Conclusion and references follow.

II. PRIOR WORK

Integration of multiple heterogenous dies on a silicon interposer achieves high interconnect density with lower power and better performance. This has motivated the recent advances in 2.5D integration and system-in-package solutions. There are few noteworthy technologies in this area. CoWoS [8] (Chip-on-Wafer-on-Substrate) has been proposed as a packaging solution comprising of ultra-thin interposers of 50µ thickness with through-silicon-vias (TSVs). Here different logic dies can be placed on the interposer connected through micro-bumps with multiple interconnect layers fabricated using TSVs. It shows better coplanarity, physical scalability with reduced TSV diameter and depth. A second generation of COWOS [9] extends the size of Si Interposer using a stitching method which can scale the width and spacing of the metal lines down to 0.4µm and 0.4µm respectively, over a large IO area.

On the other hand, EMIB [11] uses a thin die of Si with multi-layer BEOL interconnects embedded in an organic substrate. The key advantage of EMIB is there is no practical limit to the die size and eliminates the need for processing a TSV layer. The signalling rates of approximately 3Gb/s for 10mm

Work is funded by SRC JUMP and is a part of ASCENT Task 2776.037
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long EMIB channel and 6-8Gb/s for 5mm long EMIB channel have been demonstrated by Intel. The IO density is ~300 channels/mm. HIST [10], unlike an interconnect bridge used in EMIB, uses a stitch-chip with high density fine pitch wires placed between the substrate and the chiplets. The contact between the stitch chip and the chiplets is established using micro bumps. Unique compressible micro-interconnects are used to reduce the effects of non-planarity in packaging. Another face-to-face die-stacking approach is the Foveros [12]. This uses TSVs to connect the bottom-most die to the package while face-to-face connections are achieved using micro-bumps. Foveros can achieve micro bump pitch of ~50µ.

Signalling in these integration technologies continues to be an area of active research. In general, the availability of high-density IO over a large area, has motivated the use of parallel IO as a high-bandwidth solution, compared to serial IO (SERDES) that has been the workhorse for die to memory interface. Parallel IO reduces the design complexity, by allowing the clock to be forwarded along with the data and individual communication channels work at a few GHz of bandwidth, which is about 10-100X lower than the most advanced SERDES links. This results in higher energy-efficiency for data-transfer while maintaining the target data-rate. To address the signalling need in chiplet to chiplet interconnects, Intel has recently proposed Advanced Interface Bus (AIB) [13] connections, which are either with lithographically printed wires on an interposer or a bridge. The AIB protocol also uses parallel IO instead of conventional SERDES. Running each IO at a much lower speed will simplify the transmitter and receiver circuity. This paper explores the design space of signalling and channel modelling in chiplet to chiplet connections. The main contributions of the paper include (1) a comprehensive EM model of the parallel IO links to quantify the intersymbol interference and the operating margins, and (2) evaluation of the conventional NRZ signaling scheme vis-à-vis PAM4 (multilevel signaling) for achieving higher bandwidth and energy-efficiency. PAM4 has not been successful in SERDES, because of the long wires in SERDES that degrade signal margins and cause high bit-error-rate (BER) at operating voltages. However, we demonstrate that in a chiplet to chiplet interconnects over short distances (which is required in the 2.5D integrated circuits), PAM4 is indeed a competitive signalling scheme.

III. Channel Modelling

With the inherent advantages of planarity, ease of fabrication and ease of integration 2.5D integrated systems have become attractive. To model the communication channels, we invoke a coplanar microstrip model for the on-chip interconnects. This is a symmetrical structure i.e., the spacing between the microstrips (pitch) is uniform and all the channels are of equal width. The generic structure of a coplanar microstrip is depicted in Fig. 2. It has a dielectric material of height h sandwiched between the common ground plane and the conductor (channel). The substrate discontinuity of the microstrip causes the dominant mode of transmission to be quasi-TEM as a result of which intrinsic impedance Z_0, phase velocity and field variation across the channel become frequency dependent. The general design constraints for microstrip lines [1] which are consistent with the interconnect designs is given by:

$$0.1 \leq {}^{w}/_{h} \leq 10 \quad (1)$$

$$0.1 \leq {}^{s}/_{h} \leq 10 \quad (2)$$

$$1 \leq \epsilon_r \leq 18 \quad (3)$$

Here, the thickness of the conductor and the ground plane t is assumed to be 2µm and the width w is 5µm. The microstrip structure though has the aforesaid advantages, comes at a cost of higher radiation due to lower isolation and thus more cross talk. The effect of E-field coupling can be observed in Fig 3 with three cases that show the variation of magnitude of electric field on the victim channel with (a) no aggressors, (b) one aggressor and (c) two aggressors. The magnitude of coupling depends on channel length and pitch. The pitch controls the crosstalk and the channel length dictates the signal attenuation. To study their effects, the pitch is varied from 5µm to 50µm and the channel length is varied from 100µm to 1000µm. Once the model is designed in HFSS, the six-port scattering parameters in the form of touchstone files are produced for further use in the channel simulation.

IV. Transceiver System Architecture

A. Bundle Data Clock Forwarded Channels

As seen from the previous section, each of the coplanar microstrip lines act as a channel transmitting data in form of voltages from transmitter to receiver. In order to enhance the area utilization, we propose single ended data transmission as opposed to the differential mode which uses twice the number of links. The negative effects of single ended mode like simultaneous switching and reference offset can be mitigated by adjusting the voltage amplitude of the signal. Also, to minimize the energy per bit, we do not use any equalization at the transmitter or receiver. Another large percent of link power consumption occurs in the clock recovery circuits at the receiver side. Hence, we try to eliminate this by using clock forwarding which essentially allows us to design a fully parallel IO. This is a distinguishing factor in the design of current parallel chiplet to

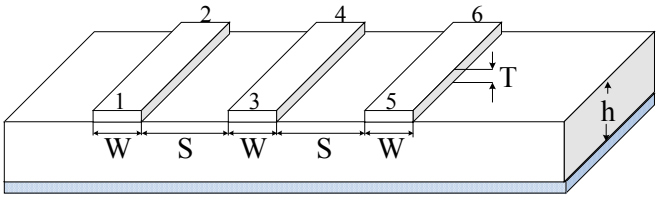

Fig. 2. Coplanar microstrip Channel Model

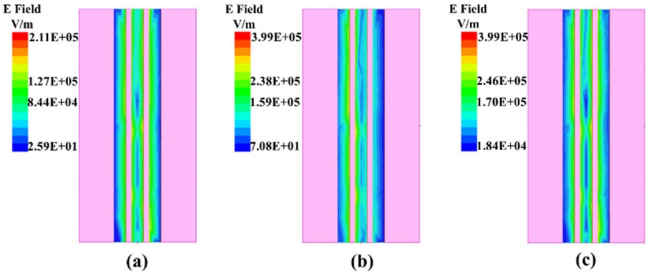

Fig. 3. E field coupling for different Scenario (a) No Aggressor Active, (b) One Aggressor Active (c) Both Aggressor Active

chiplet communication technologies and is simpler to design than traditional SERDES. This is effective because in the target designs the channel lengths are short. Thus, there can be one additional clock signal for a bundle of few data signals (8 or 16) which can be used to forward the reference clock generated on the transmitter to the receiver.

B. Signalling

In this paper, we evaluate two different signalling schemes. The circuit diagram for both are shown in Fig 4(a) and (b).

1. NRZ: The data is represented in form of single 0's and 1's. When transmitting a 0, a voltage level of 0V is sent on the channel and for transmitting a 1, a voltage of V_{dd} is sent.
2. PAM4: Here, two bits of data represent a given voltage value. The input stream of data is grouped into 2-bits and they represent the following voltage values: 00 → 0V, 01 → $V_{dd}/3$, 10 → $2V_{dd}/3$, 11→ V_{dd}. This is the linear encoding of the data bits. There can other forms of encoding like Gray codes which can be used to further reduce bit error rates. The symbol rate in either case is half that of the NRZ or in other words, the data rate in PAM4 is twice that of the symbol rate.

C. Transmitter

1. NRZ: Since we do not use any pre-emphasis or equalization, the transmitter can be as simple as a buffer which will transmit the voltages to the channel. The only design constraint for these buffers is that they must be suitably sized to be able to drive the pad capacitance of the receiver side along with that of the channel itself.
2. PAM4: Here, two bits need to be transmitted as one value of voltage. The input data is passed through a serializer which is then input to a simple 2-bit Digital to Analog Converter (DAC). The DAC will convert it to a mapped voltage and is transmitted on to the channel by a current mode driver.

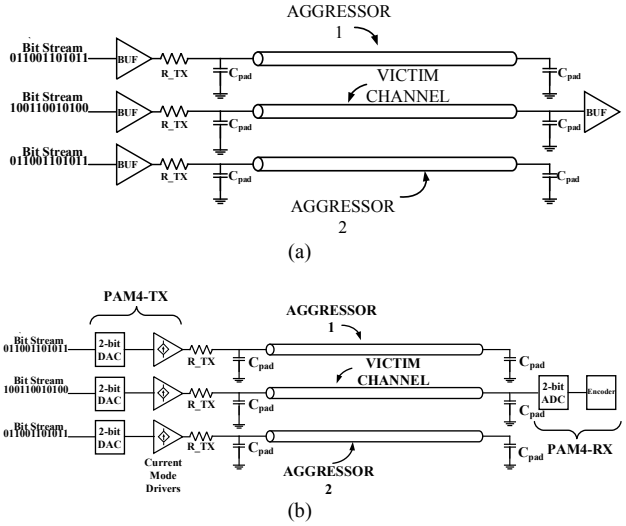

Fig. 4. Circuit of (a) NRZ Signaling (b) PAM4 Signaling

D. Receiver

1. NRZ: Much like the transmitter, the receiver can be a simple buffer which will detect the voltage on the channel and interpret it as a 0 or a 1. The buffer in this case can be viewed as a high gain voltage comparator which will compare the signal value to the trip-point voltage of the buffer in order to make the decision.
2. PAM4: The four voltage levels on the channel need to decoded back to two bits. Here, we use a simple 2-bit Analog to Digital Converter (ADC) to perform the task. Due to its speed, a flash-ADC is best suitable for the purpose. The Flash-ADC in-turn comprises of three high gain comparators which compare the signal value against the external reference voltage. The ADC output is then encoded to binary.

V. Channel Simulation

A. Simulation Setup

The simulation setup is shown in Fig 5. The simulation is performed on the Keysight Advanced Digital Systems (ADS) platform for a typical 28nm technology node. The transmitter consists of a Pseudo Random Bit Sequence generator which is electrically encoded to voltage. Here PRBS-7 is being used. The transmitter has a transmit-resistance (R-TX) typically 50Ω in shunt with the pad capacitance. The typical pad capacitance (C_{pad}) for a 28nm node is around 5pF. For the NRZ signalling, a simple buffer is used as explained in the architecture. For PAM4, we use a simplified IBIS-AMI model along with executables generated from MATLAB SERDES toolkit which can be used in conjunction with the ADS topology. For both NRZ and PAM4, we use a V_{dd} of 1V.

The channel is modelled in the form of a 6-port S-parameter network, which uses the touchstone files generated from the HFSS models. The 6 ports represent three channels, the middle victim and the outer two aggressors which contribute to the crosstalk. On the transmit side, the "XTalk" transmitters are configured to operate at the same data rate as that of the "TX" but produces an out-of-phase signal. This emulates the worst-case cross talk scenario. On the receiving side, we first encounter the pad capacitance which is again in shunt. Most conventional channels use a termination resistance. This causes the signals to attenuate which will impact the power. Thus, to reduce the power consumption, short links typically eliminate

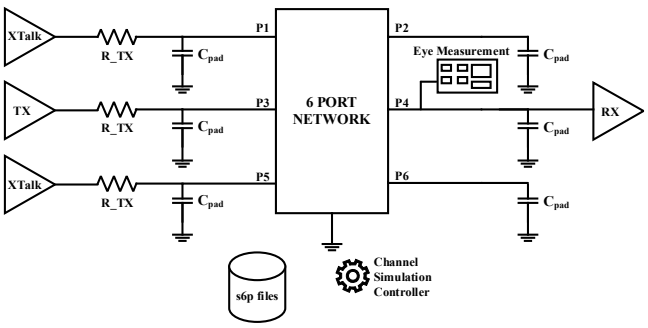

Fig. 5. Channel Simulation Setup

the legacy termination resistance as a result of which the receiver is a capacitive load. This will cause signal reflections to the transmitter in turn affecting the quality of signal and increasing inter symbol interference (ISI). Since the channels are considerably small in length the lack of termination doesn't impact the bit-error-rate (BER) significantly. The channel simulation controller performs statistical convolution of channel impulse response with that of the data transmitted and the eye-diagram is generated at the receiver side. Finally, the receiver is a simple buffer for NRZ and IBIS-AMI model for PAM4 generated from MATLAB.

B. Simulation and Measurements

The channel simulation is performed for different pitch and channel length configurations. For a given data rate, the eye-opening increases as the pitch increases and decreases as the length increases, as can be seen for typical design parameters, in Fig. 6 for NRZ and in Fig. 7 for PAM4. In an ideal case, the eye-opening must be minimum for 1000µm length- 5µm pitch channel due to highest attenuation and crosstalk and maximum for 100µm length - 50µm pitch channel due to lowest attenuation and crosstalk. But we note that the electromagnetics of the coplanar microstrip line is much more complex than

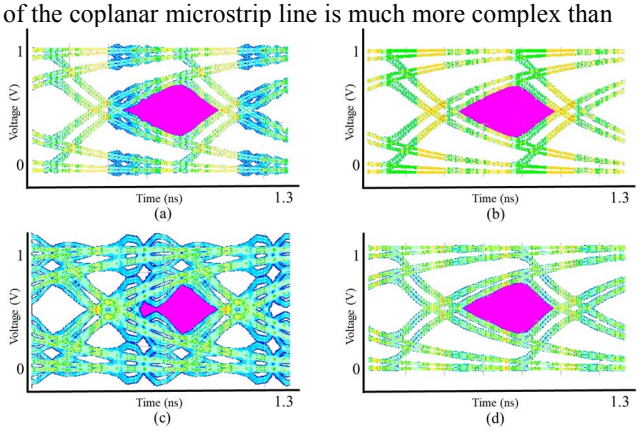

Fig. 6. NRZ Eye for (a) L=100µm, P=5µm (b) L=100µm, P=50µm (c) L=1000µm, P=5µm, (d) L=1000µm, P=50µm

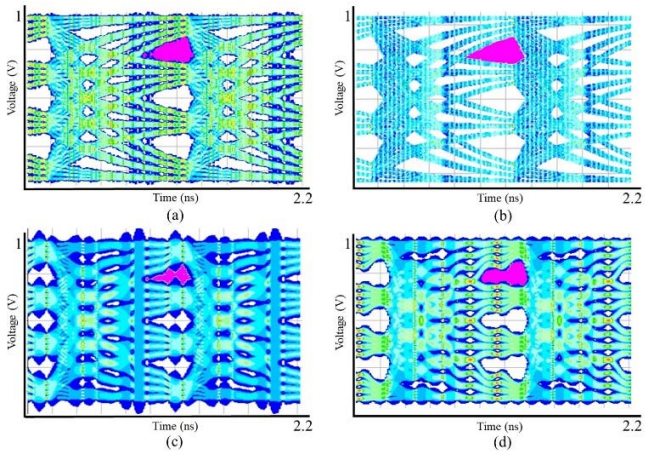

Fig. 7. PAM4 Eye for (a) L=100µm, P=5µm (b) L=100µm, P=50µm (c) L=1000µm, P=5µm, (d) L=1000µm, P=50µm

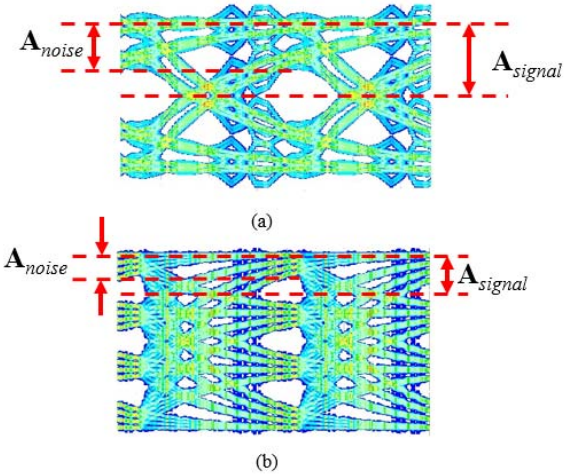

Fig. 8. COM Definition based on Eye Diagram for (a) NRZ (b) PAM4

simple linear relationships between frequency of operation and channel dimensions.

C. Channel Operating Margins and Highest Signalling Rate

The channel operating margin (COM) is a measure of channel performance which was originally developed for IEEE 802.3bj and IEEE 802.3bs Gigabit Ethernet (GbE) standards. The concept of COM has been applied for the channels under consideration. The COM is defined w.r.t the eye-diagram in Fig 8 as:

$$COM = 20log_{10}\frac{A_{signal}}{A_{noise}} \qquad (4)$$

The standard requirement for a communication channel transmitting NRZ data is that COM $\geq$ 3dB. For PAM4 signalling, since the amplitude of the ideal signal is 1/3rd that of NRZ, the target COM $\geq$ 9.5dB. In the limiting case, it will be 3dB for NRZ and 9.5dB for PAM4. For PAM4, the average of COM for all the three eyes is taken. Here in the simulation, we determine the highest data rate that can be achieved while meeting the COM requirement for every configuration of channel length and pitch. This is done by setting an optimization goal to meet the COM requirement and sweeping over a suitable frequency range. All the measurements are made for a BER of 1e-15.

Fig 9 and 10 show the intensity plot vs channel dimensions for NRZ and PAM4. The channel pitch is along the X axis and the channel length is along the Y axis. The highest data rate that can be achieved is indicated by intensity of the colour in each box.

The ideal scenario of data rate increasing with increasing channel pitch can be seen for channel length of 600µm in case of NRZ. At 40µm pitch in PAM4, the ideal trend of data rate decreasing with increasing channel length can be observed. That being said, we need to look at the general trend of the data rate as the channel dimensions are varied while considering that the maximum frequency of operation is controlled by the electromagnetics of the channel, effective dielectric constant of the substrate, characteristic impedance, resonant frequencies

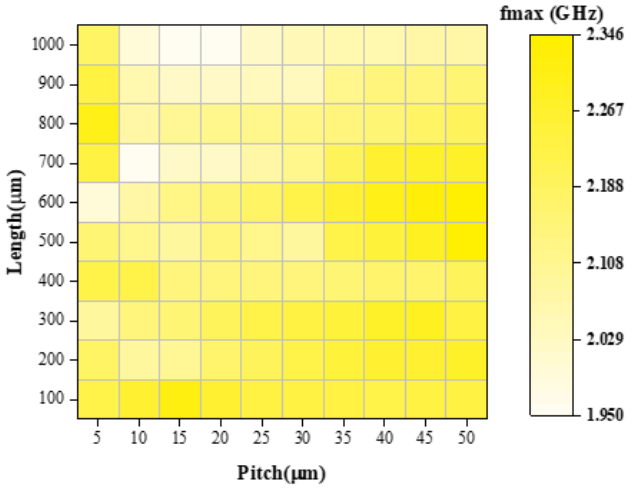

Fig. 9. Max. Freq of operation NRZ for iso-BER of 1e-15

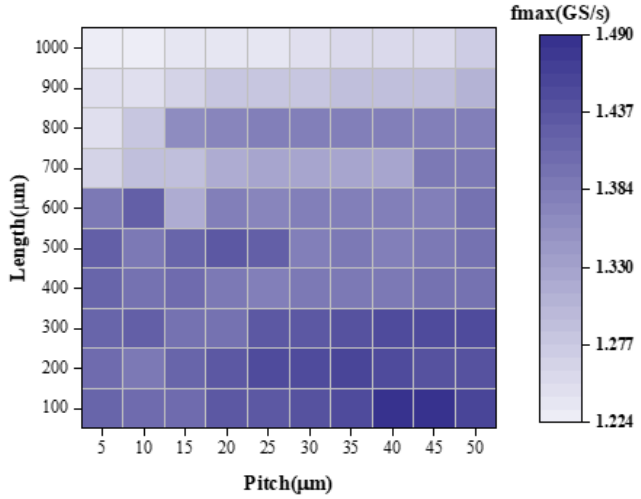

Fig. 10. Max. Freq of operation PAM4 for iso-BER of 1e-15

and so on. Traditionally channels are designed by fixing most of the physical channel parameters, but here we perform a design space exploration to identify the limits of parallel IO links.

Fig 11 and 12 show the shoreline BW density vs channel length for a sample of four pitch configurations. The direct implication of the finer pitch is increased shoreline density.

VI. Power Estimations

A. NRZ

1. TX: Assuming a single ended voltage mode transmitter, the driver is a buffer circuit which needs to drive the wire and the pad capacitance. The magnitude of wire capacitance can be neglected compared to the pad capacitance. If C_{pad} is the pad capacitance, f_{clk} is the frequency of operation, V_{dd} is the supply voltage, the power dissipation can be modelled as

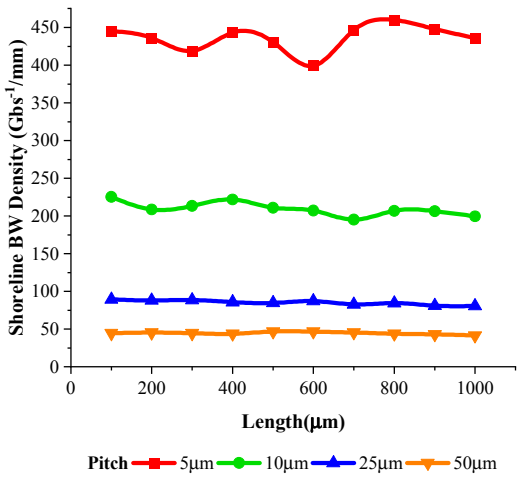

Fig. 11. NRZ Shoreline BW Density vs Channel Length

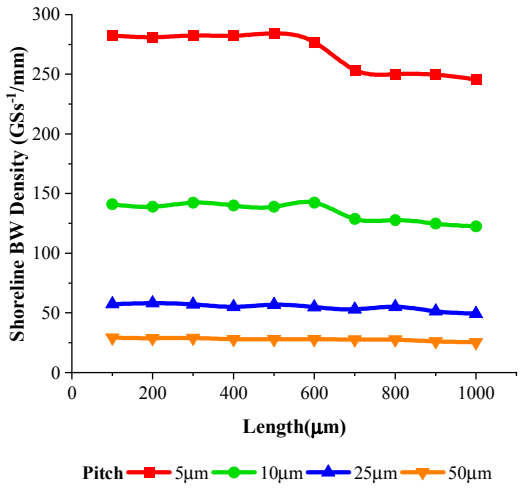

Fig. 12. PAM4 Shoreline BW Density vs Channel Length

$$P_{TX} = C_{pad} f_{clk} V_{dd}^2 \qquad (5)$$

2. RX: The single ended receiver is a buffer that decodes the signal to a 0 or 1 level and has the same power expression given by (5) but with load capacitance just another buffer.

B. PAM4

1. DAC: We consider a simple capacitive binary-weighted array DAC structure. The capacitive switching will be the key component of power consumption in this structure. [2] provides a power estimation of such structures; when applied to a 2-bit DAC with equal probability of 0's and 1's gives equation (6). f_{clk} is the frequency of operation, C_0 is the capacitance of the unit capacitor, V_{ref} is the reference voltage for the conversion. A simple current mode driver comprising of two binary weighted current sources with tail currents I_T and $2I_T$ can be utilized to drive the signal. This power is given by (7):

$$P_{DAC} = \frac{9}{32} f_{clk} C_0 V_{ref}^2 \quad (6)$$

$$P_{CMD} = 3 V_{DD} I_T \quad (7)$$

2. ADC: As mentioned, due to the speed of operation and low-resolution requirements, a Flash ADC will be the most suitable candidate. The flash ADC comprises of 2^N-1 comparators and an encoder. For a N=2-bit ADC, we need 3 comparators. The power of a matching limited comparator [3] and the Wallace encoder is given by [4] as in (8) and (9) respectively. Here C_{ox} is oxide capacitance, A_{VT} is threshold voltage mismatch coefficient, V_{inpp} is peak-to-peak input voltage, C_{Cmin} is minimum required capacitance, E_{gate} is energy of a typical gate, N is number of bits.

$$P_{Comp} = \left(144 \cdot 2^{2N} C_{ox} A_{VT}^2 \frac{V_{dd}^2}{V_{inpp}^2} + C_{c\,min} V_{dd}^2\right)(2^N - 1) f_{clk} \quad (8)$$

$$P_{enc} = 5 \cdot (2^N - N) \cdot E_{gate} \cdot f_{clk} \quad (9)$$

C. Phase Locked Loop (PLL)

We consider a non-differential 5 stage VCO along with PFD from [5]. [6] provides an elaborate power estimation treating the PLL as a 2nd order continuous time system. Given the damping factor (0.707) and natural frequency (9.375MHz) with a multiplier of N= 32, the power of a PLL can be written as (10), where C_{PFD}, C_{DIV}, C_{VCO} are the total capacitances of a Phase-Frequency Detector, Frequency Divider and Voltage Controlled Oscillator respectively. The Frequency Divider circuit is a series of TSPC Flops [7] along with TG multiplexers and inverters. P_{BIAS} is the power of the bias circuitry.

$$P_{PLL} = (C_{PFD} + C_{DIV} + C_{VCO}) \cdot V_{dd}^2 \cdot f_{clk} + P_{BIAS} \quad (10)$$

The total power for a ***2.345Gb/s*** NRZ is ***31.2mW*** leading to an energy-efficiency of ***13.323pJ/b***. For the ***1.49GS/s*** PAM system, the power is ***14.53mW*** producing an energy-efficiency of ***4.876pJ/bit***.

TABLE1. TABLE SHOWING VARIOUS PARAMETERS AND THEIR VALUES

Process Parameter	Typical Value for 28nm Node
C_{ox}	45fF/ μ m^2
A_{VT}	1.2mV- μ m
E_{gate}	1.2fJ
C_{cmin}	5fF
C_0	1pF
Others	**Value**
I_T	0.5mA
V_{inp-p}	1V
P_{bias}	0.5mW

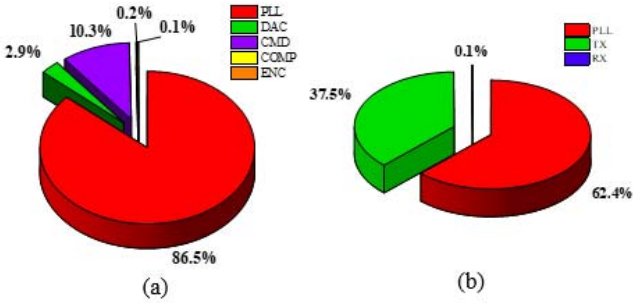

Fig 13. Power consumption of various components in (a) PAM4 (b) NRZ

Fig. 13 show the breakdown of power consumption. As expected, the PLL is the major consumer with up to 62.4% in NRZ and 86.5% in PAM. The receiver in both cases is negligible, as we do not use any equalizer or CDR. Typical process parameter values for 28nm node and other simulation variables are tabulated in Table 1.

VII. CONCLUSIONS

In this paper we explore coplanar microstrip based channels as a model for die to die interconnects for 2.5D integration. We show that higher order modulation like PAM can be applied with more than 63% energy efficiency per bit. This is enabled by the simple transceiver structures for short channel lengths. At high channel densities of up to 5µm pitch, we note that we can achieve 445Gb/s/mm of shoreline-BW-density with NRZ and 565Gb/s/mm with PAM4.

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