UVFR: A Unified Voltage and Frequency Regulator with 500MHz/0.84V to 100KHz/0.27V Operating Range, 99.4% Current Efficiency and 27% Supply Guardband Reduction

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Abstract—A fully-digital, single-loop Unified Voltage and Frequency Regulator (UVFR) is designed in 130nm CMOS to provide the correct supply to digital loads to meet a timing criteria. Simultaneously a Tunable Replica Circuit (TRC) based local oscillator is generated from the regulated supply and clocks the load. Measurements show 0.84V to 0.27V range of operation, and 27% supply guardband reduction at iso-performance through adaptation and resiliency which are intrinsic to the control loop.

Keywords—LDO, clocking, adaptation, resiliency, DVFS

I. INTRODUCTION

Fine-grained Dynamic Voltage and Frequency Scaling (DVFS) continue to pose significant challenges to power delivery, voltage regulation and clocking. Compact, power-efficient LDOs capable of supplying large load transients are being actively researched [1-4]. Similarly, advanced PLL [5] and clock distribution [6] techniques that respond to supply voltage droops have been proposed. But their effectiveness is limited. Droop sensitivity in [5] is limited by the PLL loop BW. [6] requires complex auto-tuning or calibration, high-overhead clock buffers and finely-controlled clock gating. Conventional systems are limited by the fact that voltage and frequency are generated by separate control loops. Motivated by the observation that the main objective of supply voltage regulation is meeting timing, we present a Unified Voltage Frequency Regulator (UVFR) that sets the regulation in digital systems is meeting timing, we present a UVFR system utilizes two clocks \( F_{\text{REF}} \), the reference frequency generated from a shared PLL and \( F_{\text{LOC}} \) generated from a local VCO (LVCO) that is powered by \( V_{\text{REG}} \). Fig. 2 illustrates the circuit implementation with \( N=1 \). The reference clock and the LVCO outputs are used to clock a 16-bit Johnson Counter (JC) with overrun protection [8], PWM generation and embedded output drivers.

The UVFR system utilizes two clocks \( F_{\text{REF}} \), the reference frequency generated from a shared PLL and \( F_{\text{LOC}} \) generated from a local VCO (LVCO) that is powered by \( V_{\text{REG}} \). Another 16-bit JC triggered by the negative clock edges provide further multi-phase capabilities. At steady-state condition, the phase difference between \( F_{\text{REF}} \) and \( F_{\text{LOC}} \) locks to a constant value and turns the power P-MOS "on" for the exact duration of time that the load current demands to keep \( V_{\text{REG}} \) constant. The phase locking occurs at each stage of the JC and the total current provided by all the PMOS devices in a time interleaved manner enables voltage regulation. If a load transient causes the \( V_{\text{REG}} \) to decrease from its steady state value, then the LVCO responds by slowing down \( F_{\text{LOC}} \) and stretching the pulse at \( L_i \). This perturbs the phase locking and creates additional phase difference allowing the pull up devices to supply higher current until re-locking and regulation are again achieved. Similarly, if the \( V_{\text{REG}} \) increases from its steady state value \( F_{\text{LOC}} \) speeds up, which reduces the phase difference and the loop goes out of lock. This in turn reduces the supply of current by the pull-up devices and ultimately reduces \( V_{\text{REG}} \) until re-locking is achieved. The process locks \( F_{\text{REF}} \) to \( F_{\text{LOC}} \) and a multi-phase design enables a ripple-free \( V_{\text{REG}} \).

The overrun protection (OP) circuit removes any phase aliasing in the XOR based phase detector (PD) (Fig. 3a), and its circuit implementation (Fig. 3b) consists of the logic that (a) holds the value of \( R_i \) if \( L_i=R_i \) and propagates the previous

Fig 1: Unified Voltage Frequency Regulator (UVFR) Architecture

Fig 2: Johnson Counter based multi-phase Unified Voltage Frequency Co-regulator (Here \( N=1 \))
stage value \((R_{i-1})\) to \(R_i\) if \(L_{i} \neq R_{i}\) and (b) holds the value of \(L_i\) if \(L_{i} \neq R_{i}\) and propagates the previous stage value \((L_{i-1})\) to \(L_i\) if \(L_{i} = R_{i}\). The OP block is needed to remove the locking range limitation imposed by the XOR gate based phase detector.

Instead it is able to lock the loop and operate till the maximum current limitation of the power devices. During a large load transient, when \(F_{LOC}\) slows down with respect to \(F_{REF}\), the phase difference \(F_{LOC}\) and \(F_{REF}\) saturates to \(\pi\). This implies 100% duty cycle for the pull-up devices i.e. the devices remain on throughout the cycle and provide the maximum load current possible. On the other extreme if the \(F_{LOC}\) compared to \(F_{REF}\) is high due to either a change in \(F_{REF}\) or a large negative load step, then the phase difference approaches 0. This implies that the pull devices are turned off until the output voltage decreases to restore the locking between \(F_{REF}\) and \(F_{LOC}\). It is interesting to note that the JC computes phase differences in parallel. By virtue of the fact that at any positive latch and a positive edge triggered flip-flop sample random logic) with error-detection capability (Fig. 4) where a current design, the digital load consists of a pipeline state (of the UVFR is designed to drive digital load circuits. In the current design, the digital load consists of a pipeline state (of random logic) with error-detection capability (Fig. 4) where a positive latch and a positive edge triggered flip-flop sample

The same data and produce an error signal if they are unequal – which signifies a delay induced error. The error detection window is equal to the high phase of the clock and for droops of up to 35% we can correctly capture any pipeline error. Scan programmable DC load circuits and high-speed noise generation circuits are integrated to mimic a large dynamic load range, and abrupt load steps characteristic of power gating/un-gating or power state transitions in realistic load conditions. Capability is provided through high speed pads to excite load transients as well as observe \(F_{REF}\), \(F_{LOC}\), error signals from the pipeline output and the output voltage node, \(V_{REG}\). The LVCO consists of a scan programmable non-inverting Tunable Replica Circuit (TRC) which is calibrated to mimic half the critical path delay and consists of both transistor-dominated and interconnect-dominated segments (Fig. 5(a)). It is half because 1/\(F_{REF}\) should equal to twice the TRC path delay. An inverting level shifter performs the following functions: (1) It acts as TRC timing guard-band of less than 5%. (2) It closes the TRC loop to form the LVCO and (3) it feeds the JC. The schematic diagram for the level shifter has been provided in the Fig. 5(b). At steady state, \(V_{REG}\) is at the correct voltage such that the TRC based VCO locks its frequency to \(F_{REF}\). Consequently, \(V_{REG}\) is also the correct voltage to enable the critical path of the pipeline circuit to meet the timing requirement (1/\(F_{REF}\)). The digital load is clocked by LVCO. Hence, any voltage droop (overshoot) at \(V_{REG}\) leads to LVCO slowing down (speeding up) proportional to the critical path thereby preventing delay errors in the pipeline. This leads to a larger (smaller) phase difference between \(F_{REF}\) and \(F_{LOC}\) which in turn increases (decreases) the duty cycle of power MOSFETs [8]. This brings \(V_{REG}\) back to regulation and \(F_{LOC}\) back to \(F_{REF}\) simultaneously.

To understand the system dynamics, we linearize the loop and Fig. 6 shows the small signal s-domain model of the UVFR control loop.
that the FLOC is linearly coupled to VREG. However, it should be noted that the linearity is assumed for the purpose of the small signal model only. In reality, even if FLOC changes non-linearly with VREG (which is typical for large droops), as long as the the sensitivity of the TRC and the critical path to the supply voltage are similar, the system will not let the pipeline incur a delay error. Further, any jitter on FLOC is perfectly correlated to VREG, (which dominates over any random component) and creates a VREG-FLOC pair. The design is fabricated in GF 130nm 8-M CMOS process and the UVFR occupies an active area of 0.0204mm² as shown in Fig. 7. The test-interface is a QFN package. UVFR has low calibration overhead. Instead of calibrating the supply voltage corresponding to a frequency (as in conventional DVFS), we calibrate the TRC setting corresponding to a reference frequency in UVFR at no extra cost. However, as the the sensitivity of the TRC and the critical path to the supply voltage are similar, the system will not let the pipeline incur a delay error. Further, any jitter on FLOC is perfectly correlated to VREG, (which dominates over any random component) and creates a VREG-FLOC pair. The design is fabricated in GF 130nm 8-M CMOS process and the UVFR occupies an active area of 0.0204mm² as shown in Fig. 7. The total silicon area which includes active devices, local VCO, load circuit and scan logic is 0.11 mm². The test-interface is a QFN package. UVFR has low calibration overhead. Instead of calibrating the supply voltage corresponding to a frequency (as in conventional DVFS), we calibrate the TRC setting corresponding to a reference frequency in UVFR at no extra test-time. Additionally, most current designs already employ TRC as run-time monitors, which make the design and test overhead negligible.

III. MEASUREMENT RESULTS

UVFR allows VREG to autonomously adapt to PVT while the LVCO maintains frequency locking to the reference.

![Image](https://via.placeholder.com/150)

**Fig 10:** Measured (a) voltage droop and (b) settling time for varying FREF.

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**Fig 9:** Measured scope capture showing full load step and local clock adapting to VREG changes that the FLOC is linearly coupled to VREG. However, it should be noted that the linearity is assumed for the purpose of the small signal model only. In reality, even if FLOC changes non-linearly with VREG (which is typical for large droops), as long as the the sensitivity of the TRC and the critical path to the supply voltage are similar, the system will not let the pipeline incur a delay error. Further, any jitter on FLOC is perfectly correlated to VREG, (which dominates over any random component) and creates a VREG-FLOC pair. The design is fabricated in GF 130nm 8-M CMOS process and the UVFR occupies an active area of 0.0204mm² as shown in Fig. 7. The total silicon area which includes active devices, local VCO, load circuit and scan logic is 0.11 mm². The test-interface is a QFN package. UVFR has low calibration overhead. Instead of calibrating the supply voltage corresponding to a frequency (as in conventional DVFS), we calibrate the TRC setting corresponding to a reference frequency in UVFR at no extra test-time. Additionally, most current designs already employ TRC as run-time monitors, which make the design and test overhead negligible.

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***Measurements in Fig. 8 illustrate how VREG automatically adapts to VREF all the way to the Near Threshold Voltage (NTV) operation. At FREF=100KHz and T=90C, the loop maintains regulation with VREG=270mV which is below process VT (linear VT=300mV). At FREF=500MHz and T=25C, the loop locks with VREG=0.84V. Further the loop can track temperature (Fig. 8a), process (Fig. 8b) and aging (Fig. 8c) providing just enough VREG to maintain the frequency lock and eliminating voltage guard-bands (measured: 14-32% for temperature, 30% for process, 6-7% for aging). Oscilloscope capture for a 3mA load step at FREF=400MHz (Fig. 9) shows 180ns droop recovery time and the corresponding LVCO clock cycles. However, unlike in conventional designs where the pipeline has to wait for the voltage regulator and the PLL to both settle before operation can be restarted, the UVFR, by virtue of the coupled VREF-FLOC loop allows error-free operation even under large droops.

**Fig 11:** Measured scope data on high-speed active probe shows UVFR enables error-free operation even under large droops

Measurements from oscilloscope captured data in Fig. 11 illustrate the ability of the UVFR scheme to provide resiliency to delay errors. As the VREG droops (under load step), a baseline design (where the digital load is clocked by the PLL) continues to operate without any pipeline error, demonstrating perfect compensation between clock and data and works across all frequency and voltage ranges as long as the TRC is well calibrated.

**Fig 12(a)** shows ~2mV/mA of load regulation for different FREF-VREG combinations. **Fig. 12(b)** shows ~10mV/V line regulation with corresponding frequency locking (measured as
A single-loop UVFR in 130nm CMOS has been presented. Measured data across a wide range of voltage and current inputs reveals peak current efficiency of 99.4% and 27% an average over 1000 cycles) and the concept of $F_{\text{REF}}-V_{\text{REG}}$ co-regulation. It should be noted that during these measurements, the digital load circuit was continuously clocked. In Fig. 13 current efficiency vs. load current has been shown across a wide range of reference frequencies from 10 to 500 MHz. The UVFR macro consumes $36\mu\text{A}(@F_{\text{REF}}=100\text{KHz})$ to $330\mu\text{A}(@F_{\text{REF}}=500\text{MHz})$ ($V_{\text{IN}}=1\text{V}$) and shows a peak current efficiency of 99.4%. Fig. 14 shows the measured supply-performance trade-off between the baseline design and the UVFR design. Owing to a smaller guard-band UVFR enables 18-27% reduction of $V_{\text{REG}}$ at iso-$F_{\text{REF}}$. Only the droop induced guard-band is considered here, as PVT sensors can potentially reduce voltage guard-bands in baseline designs as well.

Table 1 shows comparison of the LDO characteristics with other published results and show competitive FOMs. Table 2 compares UVFR with supply aware clocking techniques and this unique single-loop ‘clock and supply regulation’ provides inherent adaptation and resiliency resulting with significant guard-band reduction.

### IV. CONCLUSIONS

A single-loop UVFR in 130nm CMOS has been presented. Measured data across a wide range of voltage and current inputs reveals peak current efficiency of 99.4% and 27%