Arijit Raychowdhury

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Director, Georgia Tech Center for Circuits and Systems

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I. Earned Degrees

2002–2007 **Ph.D.**, *Electrical & Computer Engineering*, Purdue University, USA.

1997–2001 **B.E.**, *Electronics & Telecommunication Engineering*, Jadavpur University, India.

II. Employment History

2021-present **Motorola Solutions Foundation Professor**, *School of ECE, Georgia Tech.*, Atlanta, USA.

2019-present **Professor**, *School of ECE, Georgia Tech.*, Atlanta, USA.

2015-2019 **ON Semiconductor Jr Professor**, *School of ECE, Georgia Tech.*, Atlanta, USA.

2013-2019 **Associate Professor**, *School of ECE, Georgia Tech.*, Atlanta, USA.

2009-2010 **Visiting Lecturer**, *Electrical and Computer Engineering, Portland State University*, Portland, USA.

2010-2013 **Staff Research Scientist**, *Circuit Research, Intel Corporation*, Hillsboro, USA.

2007-2010 **Senior Research Scientist**, *Circuit Research, Intel Corporation*, Hillsboro, USA.

Summer 2006 **Graduate Student Intern**, *Circuit Research, Intel Corporation*, Hillsboro, USA.

Summer 2005 **Graduate Student Intern**, *Circuit Research, Intel Corporation*, Hillsboro, USA.

2002-2007 **Graduate Research & Teaching Assistant**, *Purdue University*, West Lafayette, USA.

2001-2002 **Analog Design Engineer**, *Texas Instruments Inc.*, Bangalore, India; Dallas, USA.

Summer 2000 **Undergraduate Student Intern**, *Texas Instruments Inc.*, Bangalore, India.

III. Honors and Awards

A. International, National Awards and Best Paper Awards

2021 **Best Paper Award**, *Custom Integrated Circuits Conference (CICC)*.

2021 **Distinguished Lecturer**, *IEEE Solid State Circuits Society*.

2020 **Best Paper Award**, *VLSI SoC Conference*.

2020 **Qualcomm Faculty Award**, *Qualcomm Technologies Inc.*.

2019 **Top Pick in Hardware Security and Embedded Systems**, *IEEE*.

2018 **Design Automation Conference (DAC) Innovator Under 40 Award**, *ACM, IEEE and ESDA*.

2018 **Roger P. Webb Outstanding Junior Faculty Award**, *Georgia Institute of Technology*.

2018 **Best in Session Award**, *SRC Techcon*.

2017 **Best Paper Award**, *IEEE Transactions on Multi-scale Computing Systems*.

2017 **Best Paper Award**, *Hardware Oriented Security and Trust (HOST)*.

2017 **Best in Session Award**, *SRC Techcon*.

2016 **Best in Session Award**, *SRC Techcon*.

2015 **Early Career Faculty Award**, *Intel Corporation*.

2015 **Best Paper in Analog and Mixed-Signal Track**, *IEEE VLSI-SoC Conference*.

2015 **ON Semiconductor Junior Professorship**, *School of ECE*, Georgia Tech.

2015 **ECE Teaching Fellow**, *School of ECE*, Georgia Tech.

2015 **CISE Research Initiation Initiative (CRII) Award**, *National Science Foundation*.

2015 **Best in Session Award**, *SRC Techcon*.

2014 **Cited in NSF Top News**, *for the paper entitled: Synchronized charge oscillations in correlated electron systems*.

2013 **Honorable Mention**, *The list of Four Decades of Multi-Valued Logic: Lists of Highly Cited Papers*.

2013 **Senior Member**, *IEEE*.

2012 **Best Paper Award**, *International Symposium on Low Power Electronic Design*.

2012 **Divisional Recognition Award**, *For contributions to "Always On" microphones, Intel*.

2011 **Technical Contribution Award**, *Intel*.

2010, 2011 **Patent Recognition Awards**, *Granted for more than seven patents in one year, Intel Corporation*.

2007 **Dimitris N. Chorafas Award**, *presented annually by the Chorafas Foundation (Switzerland) for outstanding doctoral research*.

2007 **Best Thesis Award**, *College of Engineering, Purdue University*.

2006 **Best Paper Award**, *International Symposium on Low Power Electronic Design*.

2005 **Intel Foundation Fellowship**, *Graduate Studies at Purdue University*.

2005 **SRC Technical Excellence Award**, *Research Team Member, Purdue University*.

2003 **Best Paper Award**, *IEEE Nanotechnology Conference*.

2003 **NASA INAC Fellowship**, *NASA Ames Research Center*.

2002 **Meissner Fellowship**, *Purdue University*.

2001 **B. C. Roy Gold Medal**, *First position in the College of Engineering, Jadavpur University among all Engineering Departments*.

2001 **Gold Medal**, *First position in the Department of Electrical & Telecommunication Engineering, Jadavpur University*.

2001 **Winner of Design Award**, *First position in the World DSP Meet, Texas Instruments for the paper entitled, Extended Kalman filter based target tracking in mobile robots using TMS320C2x.*

1997 **Governor's Gold Medal**, *First position in the School Leaving Examination, Std 12, in the state among 500,000+ students.*

Student Awards

2021 **Semiconductor Research Corporation Graduate Fellowship**, *Semiconductor Research Corporation*, Foroozan Karimzadeh.

2021 **NSF Graduate Fellowship**, *National Science Foundation*, Justin Ting.

2021 **Black Students in Technology Scholarship**, *Cadence*, Adou Sangbone Assoa.

2020 **Seed Research Grant**, *Oak Ridge National Labs (ORNL)*, Rakshith Saligram.

2019 **International Solid State Circuits Conference Predoctoral Research Award**, *IEEE ISSCC*, Minxiang Gong.

2019 **Top Pick in Hardware Security and Embedded Systems**, *IEEE*, Saad Bin Nasir.

2019 **Taiwan Government Scholarship to Study Abroad (GSSA)**, *Government of Taiwan*, Muya Chang.

2019 **Qualcomm Innovation Fellowship**, *Qualcomm*, Muya Chang, Brian Crafton.

2019 **Chih Foundation Graduate Research Award**, *Chih Foundation*, Muya Chang.

2018 **Chih Foundation Graduate Research Award**, *Chih Foundation*, Abhinav Parihar.

2017 **IEEE SSCS Pre-Doctoral Research Award**, *IEEE ISSCC*, Saad Bin Nasir.

2014 **Honorable Mention, Qualcomm Innovation Fellowship**, *Qualcomm*, S Gangopadhyay and S B Nasir.

IV. Research, Scholarship, and Creative Activities

A. Published Book Chapters, and Edited Volumes

A1. Refereed Book Chapters

BC1. Arijit Raychowdhury and Kaushik Roy, "Nanometer Scale Technologies: Device Considerations" in *"Nano, Quantum and Molecular Computing: Implications To High Level Design And Validation"*, Kluwer Academic Publishers, ISBN: 1402080670, June 2004.

BC2. Ali Keshavarzi and Arijit Raychowdhury, "Carbon nanotubes for digital circuits: Promises, Challenges and Outlook" in *"Carbon Nanotube Electronics (Series on Integrated Circuits and Systems)"*, ISBN-10: 0387368337 August 2008.

BC3. Amit Agarwal, Saibal Mukhopadhyay, Chris H. Kim, Arijit Raychowdhury and Kaushik Roy, "Power Estimation and Reduction" in *"System on Chip: Next Generation Electronics"*, IEE Press, ISBN: 0-86341-552-0, 2009.

BC4. Bipul Paul and Arijit Raychowdhury, "Digital Subthreshold for Ultra-Low Power Operation: Prospects and Challenges," in *"Low-Power Variation-Tolerant Design in Nanometer Silicon"*, Springer Publications, USA, October 2010.

BC5. Anvesha Amravati, Manan Chung and Arijit Raychowdhury, "A SAR Pipeline ADC with Time Interleaved DAC Sharing for Ultra-Low Power Camera Front Ends," in *"VLSI-SoC: From Systems to Chips"*, Springer Publications, USA, 2016.

BC6. N Shukla, S Datta, A Parihar, A Raychowdhury, "Computing with Coupled Relaxation Oscillators," in *Future Trends in Microelectronics: Journey Into the Unknown*, Wiley, USA, Oct, 2016.

BC7. Rakshith Saligram, Ankit Kaul, Muhannad S Bakir, and Arijit Raychowdhury, "Multilevel Signalling for High-Speed Chiplet-to-Chiplet Communication," in *"VLSI-SoC: Advanced Topic on Systems-on-Chip"*, Springer Publications, USA, 2020.

BC8. Brian Crafton, Samuel Spetalnick, Gauthaman Murali, Tushar Krishna, Sung-Kyu Lim, and Arijit Raychowdhury, "Statistical Array Allocation and Partitioning for Compute In-Memory Fabrics," in *"VLSI-SoC: Advanced Topic on Systems-on-Chip"*, Springer Publications, USA, 2020.

B. Refereed Publications and Submitted Articles

B1. Published and Accepted Journal Articles

J1. A. Raychowdhury, B. Gupta, and R. Bhattacharjee, " Bandwidth improvement of microstrip antennas through a genetic-algorithm-based design of a feed network," *Microwave and Optical Technology Letters*, Vol. 27, Issue 4, 2000, pp: 273-275.

J2. I. Saha Misra, A. Raychowdhury, K. K. Mallik, and M. N. Roy. "Design and optimization of a nonplanar multidipole array using genetic algorithms for mobile communications," *Microwave and Optical Technology Letters*, Vol. 32, Issue 4, 2002, pp:301-304.

J3. Arijit Raychowdhury, Saibal Mukhopadhyay and Kaushik Roy, "A Circuit Compatible Model of Ballistic Carbon Nanotube Field Effect Transistors", *IEEE Transactions on Computer Aided Design (TCAD)*, Vol. 23, no. 10, Oct. 2004, pp: 1411-1420. (Most downloaded paper of 2004)

J4. B. C. Paul, A. Raychowdhury, and K. Roy, "Device Optimization for Digital Subthreshold Operation," *IEEE Transactions on Electron Devices (TED)*, Vol. 52, Issue 2, Feb. 2005 pp: 237- 247.

J5. Arijit Raychowdhury and Kaushik Roy, "Carbon nanotube based voltage-mode multiple-valued logic design," *IEEE Transactions on Nanotechnology (TNANO)*, Vol. 4, Issue 2, Mar. 2005, pp: 168-179 (Featured in Forty Years of Multi-Valued Logic).

J6. Saibal Mukhopadhyay, Arijit Raychowdhury and Kaushik Roy, "Accurate Estimation of Total Leakage in Nanometer Scale Bulk CMOS Circuits Based on Device Geometry and Doping Profile," *IEEE Transactions on Computer Aided Design (TCAD)*, Vol. 24, Issue 3, Mar. 2005, pp: 363-381.

J7. Swarup Bhunia, Arijit Raychowdhury and Kaushik Roy, "Frequency Specification Testing of Analog Filters Using Wavelet Transform of Dynamic Supply Current," *Journal of Electronic Testing: Theory and Applications*, March 2005.

J8. Swarup Bhunia, Arijit Raychowdhury and Kaushik Roy, "Defect Oriented Testing of Analog Circuits Using Wavelet Analysis of Dynamic Supply Current," *Journal of Electronic Testing: Theory and Applications*, Vol. 21, Issue 2, April 2005.

J9. Myeong-Eun Hwang, Arijit Raychowdhury, and Kaushik Roy, "Energy Recovery Techniques to Reduce On-chip Power Density in Molecular Nano-Technologies", *IEEE Transactions on Circuits and Systems I (TCAS-I)*, Vol. 52, no. 8, Aug. 2005, pp: 1580-1589.

J10. Arijit Raychowdhury, Bipul Paul, Swarup Bhunia, and Kaushik Roy, "Computing with Subthreshold Leakage: Device/Circuit/Architecture Co-design for Ultralow-Power Subthreshold Operation", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 13, Issue 11, Nov. 2005, pp: 1213-1224.

J11. Arijit Raychowdhury and Kaushik Roy, "Modeling of Metallic Carbon Nanotube Interconnects for Circuit Simulations and a Comparison with Cu Interconnects for Scaled Technologies", *IEEE Transactions on Computer Aided Design (TCAD)*, Vol. 25, Issue 1, Jan. 2006, pp: 58-65.

J12. N. Banerjee, A. Raychowdhury, K. Roy, S. Bhunia, and H. Mahmoodi, "Novel Low-Overhead Operand Isolation Techniques for Low-Power Datapath Synthesis", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 14, Issue 9, Sep. 2006, pp: 1034-1039.

J13. Arijit Raychowdhury, Ali Keshavarzi, Juanita Kurtin, Vivek De, and Kaushik Roy, "Analysis of Carbon Nanotube Field Effect Transistors for High Performance Digital Logic - Modeling and DC Simulations", *IEEE Transactions on Electron Devices (TED)*, Vol. 53, Issue 11, Nov. 2006, pp: 2711-2717.

J14. Ali Keshavarzi, Arijit Raychowdhury, Juanita Kurtin, Kaushik Roy, and Vivek De, "Analysis of Carbon Nanotube Field Effect Transistors for High Performance Digital Logic – Transient Analysis, Parasitics and Scalability", *IEEE Transactions on Electron Devices (TED)*, Vol. 53, Issue 11, Nov. 2006, pp: 2718-2726.

J15. Swaroop Ghosh, Swarup Bhunia, Arijit Raychowdhury and Kaushik Roy, "A Novel Delay Fault Testing Methodology Using Low-Overhead Built-in Delay Sensor," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, Vol 25, Issue 12, Dec. 2006, pp: 2934-2943.

J16. Arijit Raychowdhury, and Kaushik Roy, "Carbon Nanotube Electronics: Design of High Performance and Low Power Digital Circuits", *IEEE Transactions on Circuits and Systems (TCAS) I*, Vol. 54, Issue 11, Nov. 2007, pp 2391-2401.

J17. A. Coker, V. Taylor, D. Bhaduri, S. Sukla, A. Raychowdhury, K. Roy, "Multi-junction Fault Tolerance Architecture for Nanoscaled Crossbar memory," *IEEE Transactions on Nanotechnology (TNANO)*, Vol. 7, Issue 2, Mar. 2008, pp: 202-208.

J18. Arijit Raychowdhury, Shekhar Borkar, Vivek De, Ali Keshavarzi and K. Roy, "Variation Tolerance in a Multi-channel Carbon Nanotube Transistor for High Speed Digital Circuits," *IEEE Transactions on Electron Devices (TED)*, Vol 56, Issue 3, Mar. 2009, pp: 383-392.

J19. Sumeet Kumar Gupta, Arijit Raychowdhury and K. Roy, "Compact models considering incomplete voltage swing in complementary metal oxide semiconductor circuits at ultralow voltages: A circuit perspective on limits of switching energy," *Journal of Applied Physics (JAP)*, Vol. 105, Issue 9, May 2009.

J20. Y. William Li, Hasnain Lakdawala, Arijit Raychowdhury, Greg Taylor, K. Soumyanath, "A 1.05V 1.6mW, 0.45°C 3σ Resolution $\Sigma\Delta$ based Temperature Sensor with Parasitic Resistance Compensation in 32nm Digital CMOS Process," *Journal of Solid State Circuits (JSSCC)*, Vol 44, Issue 12, Dec. 2009, pp: 3621-3630.

J21. Sumeet Kumar Gupta, Arijit Raychowdhury and K. Roy, "Digital Computation in Sub-Threshold Region for Ultra-Low Power Operation: A Device-Circuit-System Co-Design Perspective," *Proceedings of IEEE*, Vol. 98, Issue 2, Feb. 2010

J22. Keith A. Bowman, James W. Tschanz, Shih-Lien L. Lu, Paolo A. Aseron, Muhammad M. Khellah, Arijit Raychowdhury, Bibiche M. Geuskens, Carlos Tokunaga, Chris B. Wilkerson, Tanay Karnik, and Vivek K. De, "A 45nm Resilient Microprocessor Core for Dynamic Variation Tolerance," *Journal of Solid State Circuits (JSSC)*, Issue 12, Dec. 2010, pp: 282 - 283.

J23. Arijit Raychowdhury, Bibiche Geuskens, Keith Bowman, James Tschanz, Shih-Lien Lu, Tanay Karnik, Muhammad Khellah, Vivek De, "Tunable Replica Bits for Dynamic Variation Tolerance in 8T SRAM Arrays," *Journal of Solid State Circuits (JSSC)*, Vol. 46, Issue 4, Apr. 2011, pp: 797-805.

J24. Bowman, K.A., Tokunaga, C., Tschanz, J.W., Raychowdhury, A., Khellah, M.M., Geuskens, B.M., Lu, S.-L.L, Aseron, P.A., Karnik, T., De, V.K. , "All-Digital Circuit-Level Dynamic Variation Monitor for Silicon Debug and Adaptive Clock Control," *IEEE Transactions on Circuits and Systems (TCAS) I: Regular Papers* , Vol. 58, no.9, Sep. 2011, pp: 2017-2025.

J25. C. Augustine, A. Raychowdhury, D. Somasekhar, K. Roy, V. De, "Design Space Exploration of Typical STT MTJ Stacks in Memory Arrays in the Presence of Variability and Disturbances," *Transactions on Electron Devices (TED)*, Vol. 58, Issue 12, Dec. 2011.

J26. Arijit Raychowdhury, Carlos Tokunaga, Willem Beltman, Michael Deisher, James Tschanz, Vivek De, "A 2.3nJ/Frame Voice Activity Detector for Context-Aware Systems in 32nm CMOS," *Journal of Solid State Circuits (JSSC)*, Mar. 2013.

J27. Helia Naeimi, Charles Augustine, Arijit Raychowdhury, Shih-Lien Lu, James Tschanz,"STTRAM Scaling and Retention Failure," *Intel Technology Journal (ITJ)*, May 2013.

J28. Nikhil Shukla, Abhinav Parihar, Eugene Freeman, Hanjong Paik, Greg Stone, Vijaykrishnan Narayanan, Haidan Wen, Zhonghou Cai, Venkatraman Gopalan, Roman Engel-Herbert, Arijit Raychowdhury, Suman Datta, "Synchronized charge oscillations in correlated electron systems," *Nature Scientific Reports (SR)*, Vol. 4, April 2014.

J29. Samantak Gangopadhyay, Dinesh Somasekhar, James Tschanz, Vivek De, Arijit Raychowdhury, "A 32nm Embedded, Fully-Digital, Phase-Locked Low Dropout Regulator for Fine Grained Power Management in Digital Circuits", *Journal of Solid State Circuits (JSSC)*, Vol. 11, Nov. 2014.

J30. Abhinav Parihar, Nikhil Shukla, Suman Datta, Arijit Raychowdhury, "Exploiting Synchronization Properties of Correlated Electron Devices in a Non-Boolean Computing Fabric for Template Matching," *IEEE Journal On Emerging And Selected Topics In Circuits And Systems(JETCAS)*, Vol. 4, Dec. 2014.

J31. Abhinav Parihar, Nikhil Shukla, Suman Datta, Arijit Raychowdhury, "Synchronization of pairwise-coupled, identical, relaxation oscillators based on metal-insulator phase transition devices: A model study," *Journal of Applied Physics (JAP)*, Feb. 2015.

J32. P. Maffezzoni, L. Daniel, N. Shukla, S. Datta, A. Raychowdhury, V. Narayanan, "Modelling hysteresis in vanadium dioxide oscillators," *Electronic Letters*, Vol. 51, Issue 11, 28 May 2015, p. 819-820.

J33. Paolo Maffezzoni, Luca Daniel, N. Shukla, Suman Datta, Arijit Raychowdhury, "Modeling and Simulation of Vanadium dioxide Relaxation Oscillators," *IEEE Transactions on Circuits and System (TCAS) I: Regular Papers*, Vol.62, Issue 9, pp.2207-2215, Sept. 2015.

J34. Soham Desai, M. Shoaib and A. Raychowdhury, "An Ultra-low power, "Always-On" Camera Front-End for Posture Detection in Body Worn Cameras using Restricted Boltzman Machines," *IEEE Transactions on Multi-Scale Computing Systems (TMSCS)*, Vol. 1, Issue 4, pp: 187 - 194, Dec. 2015.

J35. Ashwin Chintaluri, S. Natarajan, Helia Naeimi and A. Raychowdhury, "Analysis of Defects and Fault models in Embedded Spin Transfer Torque (STT) MRAM Arrays," *IEEE Journal On Emerging And Selected Topics In Circuits And Systems(JETCAS)*, vol. PP, no. 99, pp. 1–11, 2016.

J36. R. Venkatesan, V. Kozhikkottu, M. Sharad, C. Augustine, A. Raychowdhury, K. Roy, A. Raghunathan, "Cache Design with Domain Wall Memories," *IEEE Transactions in Computers*, Vol. 65, Issue 4, pp: 1010-1024, 2016.

J37. Wei-Yu Tsai, X. Li, M. Jerry, B. Xie, N. Shukla, H. Liu, N. Chandramoorthy, M. Cotter, A. Raychowdhury, D. Chiarulli, S. Levitan, S. Datta, J. Sampson, N. Ranganathan, V. Narayanan, "Enabling New Computation Paradigms with HyperFET - an Emerging Device," in *IEEE Transactions on Multi-Scale Computing Systems*, Vol. 2, Issue 1, pp: 30-48, 2016. **(Award for the Best TMSCS Paper in 2016)**

J38. Sandip Roy, Yier Jin and A. Raychowdhury, "The Changing Computing Paradigm with Internet of Things: A Tutorial Introduction," *IEEE Design and Test Magazine (IEEE D&T)*, Vol. 33, Issue 2, pp: 76-96, 2016.

J39. Saad Bin Nasir, and A. Raychowdhury, "All-digital low-dropout regulator with adaptive control and reduced dynamic stability for digital load circuits," in *IEEE Transactions on Power Electronics (TPE)*, Vol. 31, Issue 12, Dec. 2016.

J40. Abhinav Parihar, Nikhil Shukla, Matt Jerry, Suman Datta and A. Raychowdhury, "Computing with Dynamical Systems Based on Insulator-Metal-Transition Oscillators," in *Nanophotonics*, Vol, 6, Issue 3, 2017.

J41. David C. Zhang, Madhavan Swaminathan, Arijit Raychowdhury and David Keezer, "Enhancing the Bandwidth of Low-Dropout Regulators Using Power Transmission Lines for High-Speed I/Os," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Vol. 7, Issue 4, 2017.

J42. Anvesha Amravati, Kyle Xu, Justin Romberg and A. Raychowdhury, "A Light-Powered Smart Camera with Compressed Domain Gesture Detection," in *IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)*, July, 2017.

J43. Abhinav Parihar, Nikhil Shukla, Matt Jerry, Suman Datta and A. Raychowdhury, "Vertex coloring of graphs via phase dynamics of coupled oscillatory networks," in *Nature Scientific Reports*, 7, 911, 2017.

J44. Ningyan Cao, Saad Nasir Shreyas Sen and A. Raychowdhury, "Self-Optimizing IoT Wireless Video Sensor Node with In-situ Data Analytics and Context-Driven Energy-Aware Real-time Adaptation," in *IEEE Transactions on Circuits and Systems I (TCAS I)*, Vol. 64, Issue 9, 2017.

J45. Matthew Jerry, Kai Ni, Abhinav Parihar, Arijit Raychowdhury, Suman Datta, "Stochastic Insulator-to-Metal Phase Transition based True Random Number Generator," in *IEEE Electron Device Letters (EDL)*, Jan, 2018.

J46. Insik Yoon and A. Raychowdhury, "Modeling and Analysis of Magnetic Field Induced Coupling on Embedded STT-MRAM Arrays," in *IEEE Transactions on Computer Aided Design (TCAD)*, Vol. 37, Issue. 2, Feb. 2018 .

J47. Saad Bin Nasir, S. Sen and A. Raychowdhury, "Switched Mode Control based Hybrid LDO for Fine-grain Power Management of Digital Load Circuits," in *IEEE Journal of Solid State Circuits (JSSC)*, Vol. 53, Issue. 2, Feb. 2018.

J48. Anvesha Amravati, Kyle Xu, Justin Romberg and A. Raychowdhury, "A 130nm 165nJ/frame Compressed-Domain Smashed-Filter Based Mixed-Signal Classifier for "In-sensor" Analytics in Smart Cameras," in *IEEE Transactions on Circuits and Systems II (TCAS-II)*, Vol. 65, Issue. 3, March 2018.

J49. Saad Bin Nasir, Shreyas Sen, Arijit Raychowdhury, "A Reconfigurable Hybrid Low Dropout Voltage Regulator for Wide-Range Power Supply Noise Rejection and Energy-Efficiency Trade-off," in *IEEE Transactions on Circuits and Systems II (TCAS-II)*, DOI: 10.1109/TCSII.2018.2816949, March 2018.

J50. Ningyuan Cao, Shreyas Sen, Arijit Raychowdhury, "Smart sensing for HVAC control: Collaborative intelligence in optical and IR cameras," in *IEEE Transactions on Industrial Electronics (TIE)*, DOI: 10.1109/TIE.2018.2818665, March 2018.

J51. Debayan Das, Shovan Maity, Saad Bin Nasir, Santosh Ghosh, Arijit Raychowdhury, Shreyas Sen, "ASNI: Attenuated Signature Noise Injection for Low-Overhead Power Side-Channel Attack Immunity," in *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS I)*, DOI: 10.1109/TCSI.2018.2819499, April 2018.

J52. Abhinav Parihar, Matthew Jerry, Suman Datta, Arijit Raychowdhury, "Stochastic IMT (insulator-metal-transition) neurons: An interplay of thermal and threshold noise at bifurcation," in *Frontiers of Neurosciences*, DOI=10.3389/fnins.2018.00210, April 2018.

J53. B. Chatterjee, N. Cao, A. Raychowdhury and S. Sen, "Context-Aware Intelligence in Resource-Constrained IoT Nodes: Opportunities and Challenges," in *IEEE Design and Test*, vol. 36, no. 2, pp. 7-40, April 2019.

J54. Brian Crafton, Abhinav Parihar, Evan Gebhardt and Arijit Raychowdhury, "Direct Feedback Alignment With Sparse Connections for Local Learning," in *Frontiers of Neuroscience*, May, 2019.

J55. Y. Fang, J. Gomez, Z. Wang, S. Datta, A. I. Khan, A. Raychowdhury, "Neuro-mimetic Dynamics of a Ferroelectric FET Based Spiking Neuron," in *IEEE Electron Device Letters*, Vol. 40, Iss. 7, pp. 1213-1216, July 2019.

J56. Y. Fang, Y. Fang, Z. Wang, J. Gomez, S. Datta, A. I. Khan, A. Raychowdhury, "A Swarm Optimization Solver based on Ferroelectric Spiking Neural Networks," in *Frontiers in Neuroscience*, July 2019.

J57. Yoon, Insik, Chang, Muya, Ni, Kai, Jerry, Matthew, Gangopadhyay, Samantak, Gus Smith, Hamam, Tomer, Vijaykrishnan, Narayanan, Romberg, Justin , Khan, Asif , Datta, Suman and Raychowdhury, Arijit, "A FerroFET based in-memory processor for solving distributed and iterative optimizations via least-squares method," in *IEEE Journal on Exploratory Solid-State Computational Device and Circuits (JXCDC)*, June 2019.

J58. Anupam Golder, Debayan Das, Josef Danial, Santosh Ghosh, Shreyas Sen, Arijit Raychowdhury, "Practical Approaches Toward Deep-Learning-Based Cross-Device Power Side-Channel Attack," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, July 2019, DOI: 10.1109/TVLSI.2019.2926324.

J59. B. Bhar, A. Khanna, A. Parihar, S. Datta and A. Raychowdhury "Stochastic Resonance in Insulator-Metal-Transition Systems" in *Nature Scientific Reports 10*, 5549 (2020). https://doi.org/10.1038/s41598-020-62537-3

J60. Sourav Dutta, Abhinav Parihar, Abhishek Khanna, Jorge Gomez, Wriddhi Chakraborty, Matthew Jerry, Benjamin Grisafe, Arijit Raychowdhury and Suman Datta, "Programmable coupled oscillators for synchronized locomotion," in *Nature Communications*, 10, Article number: 3299, Aug 2019.

J61. Yoon, Insik, Anwar, Malik Aqeel, Joshi, Rajiv, Rakshit, Titash and Arijit Raychowdhury, "A Hierarchical Memory System with STT-MRAM and SRAM to Support Transfer and Real-time Reinforcement Learning in Autonomous Drones," in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, Aug 2019.

J62. Ningyuan Cao, Muya Chang, Arijit Raychowdhury, "A 65-nm 8-to-3-b 1.0-0.36-V 9.1-1.1-TOPS/W Hybrid-Digital-Mixed-Signal Computing Platform for Accelerating Swarm Robotics," in *Journal of Solid State Circuits*, August 2019, DOI: 10.1109/JSSC.2019.2935533.

J63. Keith Bowman, Samantak Gangopadhyay, Francois Atallah, Hoan.H.Nguyen, Jihoon Jeong, Daniel Yingling, Amer Cassier, Brad Appel, Arijit Raychowdhury, "A 7nm All-Digital Leakage-Current-Supply Circuit for Analog LDO Dropout Voltage Reduction," in *Solid State Circuits Letters*, October 2019, DOI: 10.1109/LSSC.2019.2947239.

J64. A. Anwar and A. Raychowdhury, "Autonomous Navigation via Deep Reinforcement Learning for Resource Constraint Edge Nodes Using Transfer Learning," in *IEEE Access*, vol. 8, pp. 26549-26560, 2020, doi: 10.1109/ACCESS.2020.2971172.

J65. Muya Chang, Li-Hsiang Lin , Justin Romberg, Arijit Raychowdhury, "OPTIMO: A 65nm 279GOPS/W 16b Programmable Spatial-Array-Processor with On-Chip Network for Solving Distributed Optimizations via the Alternating Direction Method of Multipliers," in *Journal of Solid State Circuits*, vol. 55, no. 3, pp. 629-638, March 2020, doi: 10.1109/ JSSC.2019.2953831.

J66. Brian Crafton, Samuel Spetalnik, Yan Fang, and Arijit Raychowdhury, "Merged Logic and Memory Fabrics for Accelerating Machine Learning Workloads," in *IEEE Design and Test*, doi: 10.1109/ MDAT.2020.3016587.

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C87. Samantak Gangopadhyay and A. Raychowdhury, "A Quad-Output Elastic Switched Capacitor Converter and Per-Core LDO with 87% Power Efficiency and 150% Core-Frequency Range Improvement," *SRC TECHCON*, Sept, 2017.

C88. Saad B. Nasir and A. Raychowdhury, "A Reconfigurable Hybrid Low Dropout Voltage Regulator for Wide-Range Power Supply Noise Rejection and Energy-Efficiency Trade-off," *SRC TECHCON*, Sept, 2017. **(Best in Session Award)**.

C89. Anvesha Amravati and A. Raychowdhury, "A 65nm 360nA 0.4V Linear Classifier Using Time-Based Matrix-Multiplying ADC with in-situ Learning of ADC Non-Linearity," Proceedings of *Asian Solid State Circuits Symposium*, Nov, 2017.

C90. Anvesha Amravati, Kyle Xu, Justin Romberg and A. Raychowdhury, "A 65nm Compressive-Sensing Time-Based ADC with Embedded Classification and INL-Aware Training for Arrhythmia Detection," Proceedings of *IEEE Biomedical Circuits and Systems (BioCAS) Conference*, Nov, 2017.

C91. A. Parihar, Matt Jerry, Nikhil Shukla, Suman Datta and A. Raychowdhury, "Connecting Spectral Techniques for Graph Coloring and Eigen Properties of Coupled Dynamics: A Pathway for Solving Combinatorial Optimizations," Proceedings of *IEEE International Conference on Computer Aided Design (ICCAD)*, Nov, 2017.

C92. Said Hamdioui, Peyman Pouyan, Huawei Li, Ying Wang, Arijit Raychowdhury, Insik Yoon, "Test and Reliability of Emerging Non-Volatile Memories," Proceedings of *IEEE Asian Test Symposium (ATS)*, Nov, 2017.

C93. Anvesha A, Saad Bin Nasir, Sivaram Thangadurai, Insik Yoon and Arijit Raychowdhury, "A 55nm Time-Domain Mixed-Signal Neuromorphic Accelerator with Stochastic Synapses and Embedded Reinforcement Learning for Autonomous Micro-Robots" Proceedings of *International Solid State Circuits Conference (ISSCC)*, Feb, 2018.

C94. G. Csaba, A. Raychowdhury, W. Porod, S. Datta, "Computing with Coupled Oscillators: Theory, Devices, and Applications," Proceedings of *International Symposium on Circuits and Systems (ISCAS)*, May, 2018.

C95. Saad B Nasir, Swaminathan Madhavan, Arijit Raychowdhury, "A 65nm, 1.15-0.15V, 99.99% Current-Efficient Digital Low Dropout Regulator with Asynchronous Non-Linear Control for Droop Mitigation," Proceedings of *International Symposium on Circuits and Systems (ISCAS)*, May, 2018.

C96. Insik Yoon, Muya Chang, Samantak Gangopadhyay, Kai Ni, Matthew Jerry, Gus Smith, Tomer Hamam, Vijaykrishnan Narayanan, Justin Romberg, Shih-Lien Lu, Suman Datta and Arijit Raychowdhury, "A FeFET Based Processing-In-Memory Architecture for Solving Distributed Least-Square Optimizations," Proceedings of the *Device Research Conference (DRC)*, June, 2018.

C97. M. A. Anwar and A. Raychowdhury, "NavREn-Rl: Learning to fly in real environment via end-to-end deep reinforcement learning using monocular images," in *International Conference on Mechatronics and Machine Vision in Practice (M2VIP)*, 2018, pp. 1-6.

C98. Muya Chang and Arijit Raychowdhury, "A Systolic Architecture for Iterative Dynamical Systems with Application to Distributed Least Square Optimization," *SRC TECHCON*, Sept, 2018.

C99. Zheng Wang, Brian Crafton, Jorge Gomez, Ruijuan Xu, Aileen Luo, Zoran Krivokapic, Lane Martin, Suman Datta, Arijit Raychowdhury, Asif Islam Khan, "Experimental demonstration of ferroelectric spiking neurons for unsupervised clustering," in *Proceedings of the International Electron Device Meeting (IEDM)*, Dec, 2018.

C100. N. Cao, M. Chang and A. Raychowdhury, "A 65nm 1.1-to-9.1TOPS/W Hybrid-Digital-Mixed-Signal Computing Platform for Accelerating Model-Based and Model-Free Swarm Robotics," in *IEEE International Solid- State Circuits Conference, (ISSCC)*, San Francisco, CA, USA, 2019, pp. 222-224.

C101. Francois Atallah, Keith Bowman, Hoan Nguyen, Jihoon Jeong, Daniel Yingling, Yu Sun, Brad Appel, Anthony Polomik, Mahesh Harinath, Joshua Morelli, Thomas Moore, Nathaniel Reeves, Amer Cassier, Arijit Raychowdhury, "A 7nm All-Digital Unified Voltage and Frequency Regulator Based on a High-Bandwidth 2-Phase Buck Converter with Package Inductors," in *IEEE International Solid- State Circuits Conference, (ISSCC)*, San Francisco, CA, USA, 2019.

C102. M. Chang, L. Lin, J. Romberg and A. Raychowdhury, "OPTIMO: A 65nm 270MHz 143.2mW Programmable Spatial-Array-Processor with a Hierarchical Multi-cast On-Chip Network for Solving Distributed Optimizations," in *Custom Integrated Circuits Conference*, April 2019.

C103. M. Chang, S. Gangopadhyay, T. Hamam, J. Romberg and A. Raychowdhury, "Efficient Signal Reconstruction via Distributed Least Square Optimization on a Systolic FPGA Architecture," ICASSP 2019.

C104. I. Yoon, Malik Aqeel Anwar, Titash Rakshit and Arijit Raychowdhury, "Transfer and Online Reinforcement Learning in STT-MRAM Based Embedded Systems for Autonomous Drones," in *Design, Automation and Test in Europe Conference and Exhibition (DATE)*, Feb 2019.

C105. Patsy Cadareanu, CG Almudever, A Khanna, A Raychowdhury, S Datta, K Bertels, V Narayanan, M Di Ventra, P-E Gaillardon, "Rebooting our computing models," in *Design, Automation and Test in Europe Conference and Exhibition (DATE)*, Feb 2019.

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C107. Keith Bowman, Samantak Gangopadhyay Francois Atallah, Hoan Nguyen, Jihoon Jeong, Dan Yingling, Anthony Polomik, Mahesh Harinath, Nat Reeves, Amer Cassier, Brad Appel, and Arijit Raychowdhury, "A 7nm Leakage-Current-Supply Circuit for LDO Dropout Voltage Reduction," in *Symposium on VLSI Circuits*, June, 2019, DOI: 10.23919/VLSIC.2019.8778148.

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C109. B. Crafton, M. West, P. Basnet, E. Vogel, and A. Raychowdhury, "Local learning in RRAM neural networks with sparse direct feedback alignment," in *Proceedings of the International Symposium on Low Power Electronics and Design*, July 2019.

C110. Wriddhi Chakraborty, Kai Ni, Jeffrey Smith, Arijit Raychowdhury, Suman Datta, "An Empirically Validated Virtual Source FET Model for Deeply Scaled Cool CMOS," in *Proceedings of International Electron Device Meeting (IEDM)*, Dec. 2019.

C111. Debayan Das, Josef Danial, Anupam Golder, Nirmoy Modak, Shovan Maity, Baibhab Chatterjee, Donghyun Seo, Muya Chang, Avinash Varna, Harish Krishnamurthy, Sanu Mathew, Santosh Ghosh, Arijit Raychowdhury, Shreyas Sen, "EM and Power SCA-Resilient AES-256 in 65nm CMOS Through $> 350\times$ Current-Domain Signature Attenuation," in *Proceedings of IEEE International Solid- State Circuits Conference, (ISSCC)*, Feb 2020.

C112. Jong-Hyeok Yoon, and A. Raychowdhury, "A 65nm 8.79TOPS/W 23.82mW Mixed-Signal Oscillator-Based NeuroSLAM Accelerator for Applications in Edge Robotics," in *Proceedings of IEEE International Solid- State Circuits Conference, (ISSCC)*, Feb 2020.

C113. Yan Fang, Zheng Wang, Asif Khan, and A. Raychowdhury, "Ferroelectric Spiking Neural Networks," in *Proceedings of GOMACTech*, March 2020.

C114. Ashwin Lele, Yan Fang, Justin Ting and A. Raychowdhury, "Learning to Walk: Spike Based Reinforcement Learning for Hexapod Robot Central Pattern Generation," in *Proceedings of AI Circuits and Systems Conference*, March 2020.

C115. Aqeel Anwar, Titash Rakshit and A. Raychowdhury, "XbarOpt- Enabling ultra-pipelined, Novel STT MRAM Based processing-in-Memory DNN Accelerator," in *Proceedings of AI Circuits and Systems Conference*, March 2020.

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C117. S. Gangopadhyay, J. W. Tschanz and A. Raychowdhury, "A Quad-Output Elastic Switched Capacitor Converter and Per-Core LDO with 87% Power Efficiency and $2.5\times$ Core-Frequency Range Improvement," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, Sevilla, 2020, pp. 1-5, doi: 10.1109/ISCAS45731.2020.9180717.

C118. F. Karimzadeh, N. Cao, B.Crafton, J. Romberg and A. Raychowdhury, "Hardware-aware Pruning of DNNs using LFSR-Generated Pseudo-Random Indices," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2020.

C119. Justin L. Ting, Fang Yan, Ashwin Sanjay Lele and Arijit Raychowdhury, "Bio-inspired Gait Imitation of Hexapod Robot using Event-Based Vision Sensor and Spiking Neural Network," in *International Joint Conference on Neural Networks (IJCNN)*, July 2020.

C120. Foroozan Karimzadeh, Arijit Raychowdhury, "Memory and Energy Efficient Method Toward Sparse Neural Network Using LFSR Indexing," in *IEEE/IFIP International Conference on VLSI-SoC*, October 2020.

C121. Rakshith Saligram, Ankit Kaul, Muhannad S Bakir and Arijit Raychowdhury, "A Model Study of Multilevel Signaling for High-Speed Chiplet-to-Chiplet Communication in 2.5D Integration," in *IEEE/IFIP International Conference on VLSI-SoC*, October 2020.

C122. Ashwin Sanjay Lele, Yan Fang, Justin Ting, Arijit Raychowdhury, "Online Reward-Based Training of Spiking Central Pattern Generator for Hexapod Locomotion," in *IEEE/IFIP International Conference on VLSI-SoC*, October 2020.

C123. Brian Crafton, Samuel Spetalnick, Gauthaman Murali, Tushar Krishna, Sung-Kyu Lim and Arijit Raychowdhury, "Breaking Barriers: Maximizing Array Utilization for Compute In-Memory Fabrics," in *IEEE/IFIP International Conference on VLSI-SoC*, October 2020. **(Best Paper Award)**

C124. A. S. Lele, Y. Fang, J. Ting and A. Raychowdhury, "Learning to Walk: Spike Based Reinforcement Learning for Hexapod Robot Central Pattern Generation," in *2nd IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS)*, Genova, Italy, 2020, pp. 208-212, doi: 10.1109/AICAS48895.2020.9073987. **(Nominated for Best Paper Award)**

C125. Anupam Golder, Baogeng Ma, Debayan Das, Josef Danial, Shreyas Sen, Arijit Raychowdhury, "Efficient Electromagnetic Side Channel Analysis by Probe Positioning using Multi-Layer Perceptron," in *IACR Cryptol. ePrint Arch.*, 2020.

C126. M. Gong, X. Zhang and A. Raychowdhury, "Non-isolated 48V-to-1V Heterogeneous Integrated Voltage Converters for High Performance Computing in Data Centers," in *IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, Springfield, MA, USA, 2020, pp. 411-414, doi: 10.1109/MWSCAS48704.2020.9184442.

C127. H Ye, J Gomez, W Chakraborty, S Spetalnick, S Dutta, K Ni, A Raychowdhury, S Datta, "Double-Gate W-Doped Amorphous Indium Oxide Transistors for Monolithic 3D Capacitorless Gain Cell eDRAM," in *International Electron Device Meeting (IEDM)*, Dec. 2020.

C128. Jong-Hyeok Yoon, Muya Chang, Win-San Khwa, Yu-Der Chih, Meng-Fan Chang and Arijit Raychowdhury, "A 40nm 64Kb 56.67 TOPS/W Read-Disturb-Tolerant Compute-in-Memory/Digital RRAM Macro with Active-Feedback-based Read and in-situ Write Verification," in *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, 2021.

C129. B. Crafton, S. Spetalnick and A. Raychowdhury, "Merged Logic and Memory Fabrics for AI Workloads," in *Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2021, pp. 305-310.

C130. Jong-Hyeok Yoon, Muya Chang , Win-San Khwa , Yu-Der Chih , Meng-Fan Chang , Arijit Raychowdhury, "A 40nm 100Kb 118.44TOPS/W Ternary-weight Compute- in-Memory RRAM Macro with Voltage-sensing Read and Write Verification for reliable multi-bit RRAM operation," in *Custom Integrated Circuits Conference (CICC)*, 2021. **(Best Paper Award)**

C131. Rakshith Saligram , Divya Prasad , David Pietromonaco , Arijit Raychowdhury , Brian Cline, "A 64-Bit Arm CPU at Cryogenic temperatures: Design Technology Co-Optimization for Power and Performance ," in *Custom Integrated Circuits Conference (CICC)*, 2021.

C132. Rakshith Saligram , Suman Datta , Arijit Raychowdhury, "CryoMem: A 4K-300K 1.3GHz eDRAM Macro with Hybrid 2T-Gain-Cell in a 28nm Logic Process for Cryogenic Applications," in *Custom Integrated Circuits Conference (CICC)*, 2021.

C133. B. Crafton, A. Raychowdhury and S.-K. Lim, "Automatic Generation of Translators for Packet-Based and Emerging Protocols," in *International Symposium on Quality Electronic Design (ISQED)*, 2021, pp. 488-495.

C134. Tian Gao, Zishen Wan, Yuyang Zhang, Bo Yu, Yanjun Zhang, Shaoshan Liu, Arijit Raychowdhury, "iELAS: An ELAS-Based Energy-Efficient Accelerator for Real-Time Stereo Matching on FPGA Platform," in *Artificial Intelligence Circuits and Systems (AICAS)*, June 2021.

C135. Zishen Wan, Yuyang Zhang, Arijit Raychowdhury, Bo Yu, Yanjun Zhang, Shaoshan Liu, "An Energy-Efficient Quad-Camera Visual System for Autonomous Machines on FPGA Platform," in *Artificial Intelligence Circuits and Systems (AICAS)*, June 2021.

C136. Foroozan Karimzadeh, Arijit Raychowdhury, "Bitsp-Net: An efficient DNN accelerator toward bit level sparsity and compute in memory scheme," in *SRC TECHCON*, 2021.

C137. W. Chakraborty, K. A. Aabrar, J. Gomez, R. Saligram, A. Raychowdhury, P. Fay and S. Datta, "Cryogenic RF CMOS on 22nm FDSOI Platform with Record fT=495GHz and fMAX=497GHz," in *VLSI Technology Symposium (VLSI-T)*, July 2021.

C138. Brian Crafton, Sam Spetalnick, Jong-Hyeok Yoon, "Statistical Optimization of Compute In-Memory Performance Under Device Variation," in *International Symposium on Low Power Electronics and Design (ISLPED)*, July, 2021.

C. Other Publications and Creative Products

C1. Software

S1. "PETE: Purdue Emerging Technology Evaluator,"
http://nanohub.org/tools/pete/

Short Description: PETE was designed to evaluate any novel three terminal transistor for circuit level metrics. It used techniques for faster convergence and can also use incomplete, discontinuous and non-differential data points, which are often obtained experimentally. By providing a simple graphical interface and allowing researchers to provide tabulated I-V values for their experimental devices, this tool is useful for device scientists, material scientists and circuit designers. Due to its ease of use and success in correctly predicting circuit level performance of several key transistor technologies, this tool was used as the benchmarking tool in the SRC and Federal Govt. sponsored, multi-university program, namely the Nanoelectronics Research Initiative (NRI) Program. All researchers in the NRI community used this tool to evaluate their respective devices against other technologies. Currently, this tool has 510+ users, and has logged more than 21.5K simulation runs.

S2. "PEDRA: Programmable Engine for Drone Reinforcement Learning,"
https://github.com/aqeelanwar/PEDRA

Short Description: PEDRA is a Virtual Reality (VR) based programmable engine for Drone Reinforcement Learning (RL) applications. It is a test-bed for researchers to explore new learning algorithms as well as evaluate their power and performance cost for autonomous navigation. It features a VR environment build on top of the Unreal gaming engine, uses AirSim to connect to a back-end AI simulator. It is fully programmable, supports the exact dynamics of a suite of commercially available drones and features a rich set of indoor and outdoor environments for training and testing. PEDRA is currently the only available VR platform that supports distributed and federated learning across a swarm of drones. PEDRA is currently used by several research groups in both industry and academia, including researchers from Intel, Samsung, Qualcomm, Georgia Tech, Harvard, Purdue, UPenn, Penn State, IIT Delhi, UW Washington, and is used as an AI simulation platform in the SRC/DARPA JUMP Program.

C2. Patents

P1. Arijit Raychowdhury, Ali Keshavarzi, J. Kurtin, Vivek De, "Methods of forming carbon nanotube transistors for high speed circuit operation and structures formed thereby," US 11/648,209, 2006.

P2. Sandeep Oswal, Arijit Raychowdhury, Prakash E., Fernando Mujica, "DSL modem and method for reducing transmit echo therein," European Patent EP1333591, 2006.

P3. Sandeep Oswal, Arijit Raychowdhury, Prakash E., Fernando Mujica, "Adaptive Cancellation Network System And Method For Digital Subscriber Line", US Patent no. 7298838, 2007.

P4. S. Bhunia, H. Mahmoodi, A. Raychowdhury, S. Mukhopadhyay, K. Roy, "Low Power Scan Design and Delay Fault Testing Using First Level Supply Gating," US Patent no. 317319343, 2008.

P5. H. Lakhdawala, William Li, Gregory Taylor, Krishnamurthy Soumyanath, Arijit Raychowdhury, "Thermal Sensor Device," 8,096,707, 2008.

P6. Dia Khalil, Arijit Raychowdhury, Muhammad Khellah, Ali Keshavarzi, "Leakage Compensation Circuit for Dynamic Random Access Memory Cells," US 7,961,498, 2008.

P7. Muhammad Khellah, B. Gueskens, Arijit Raychowdhury, "Method and System to Lower the Minimum Operating Voltage of a Memory Array," US 8,094,505, 2009.

P8. Mark Budnik, Arijit Raychowdhury, Aditya Bansal and Kaushik Roy, "High Density Capacitors for Integrated Circuit Technologies", US Patent no. 20070171594, 2009.

P9. Jaydeep Kulkarni, M. Khellah, B. Gueskens, Arijit Raychowdhury, T. Karnik, V. De, "Memory Write Operation Methods and Circuits," US 12/823,642, 2010.

P10. Arijit Raychowdhury, J. Kulkarni, James Tschanz, "Multi-Supply Sequential Logic Unit," US 101143110, 2010.

P11. Brian Doyle, Arijit Raychowdhury, Yong Ju, Charles Kuo, Oguz Kaan, David Kencke, R. Chau, R. Golizadeh, "Memory with Elements Having Two Stacked Magentic Tunneling Junctions Devices," PCT/ US2011/ 066979, 2011.

P12. Arijit Raychowdhury, J. Kulkarni, James Tschanz, "Multi-Supply Sequential Logic Unit," PCT/ US2011/ 064848, 2011.

P13. Arijit Raychowdhury, J. Kulkarni, James Tschanz, "Apparatus, method and system for reducing clock-to-output delay of a multi-supply sequential logic unit in a processor," TW-I483092B, 2012.

P14. Charles Kuo, B. Doyle, Arijit Raychowdhury, R. Golizadeh, Oguz Kaan, "Balancing Energy Barrier Between States in Perpendicular Magnetic Tunnel Junctions," PCT/ US2011/ 068158, 2011.

P15. Marco Beltman, Matias Zanartu, Arijit Raychowdhury, Anand Rangarajan, Michael Deisher, "Speech Audio Processing," US 10-2012-7031843, 2011.

P16. Marco Beltman, Matias Zanartu, Arijit Raychowdhury, Anand Rangarajan, Michael Deisher, "Speech Audio Processing Device," PCT/US2011/042515, 2011.

P17. Marco Beltman, Matias Zanartu, Arijit Raychowdhury, Anand Rangarajan, Michael Deisher, "Speech processing apparatus and electronic device ," TW-I455112-B, 2012.

P18. Jaydeep Kulkarni, M. Khellah, B. Gueskens, Arijit Raychowdhury, T. Karnik, V. De, "Memory Write Operation Methods and Circuits," PCT/US2011/040458, 2011.

P19. Arijit Raychowdhury, Marco Beltman, James Tschanz, Carlos Tokunaga, Mike Deisher, Tomas Walsh, "Low Power Voice Detection," PCT/US2011/063622, 2011.

P20. Arijit Raychowdhury, Charles Augustine, James Tschanz, Vivek De, " Digital Clamp for State Retention," US9484917, 2012.

P21. Arijit Raychowdhury, James Tschanz, Vivek De, "Spin Transfer Torque Based Memory Elements for Programmable Device Arrays," PCT/US2012/031371, 2012.

P22. Arijit Raychowdhury, James Tschanz, Vivek De, "Spin Transfer Torque based memory elements," TW-201508743-A, 2012.

P23. Arijit Raychowdhury, Dinesh Somasekhar, James Tschanz, Vivek De, "Digitally Phase Locked Low Drop-out Regulator," PCT/US2012/057066, 2012.

P24. Arijit Raychowdhury, B. Doyle, David Kencke, Charles Kuo, James Tschanz, Fatih Hamazaoglu, Eric Wang, R. Golizadeh, "Methods and Systems to Read a Magnetic Tunnel Junction Based Memory Cell Based on a Pulsed Read Current," PCT/US2012/030490, 2012.

P25. D. Zhang, Madhavan Swaminathan, Arijit Raychowdhury, "System and method for enhancing bandwidth of low-dropout regulators using power transmission lines for high speed input output drivers," US-10712759-B2, 2018.

P26. Saad Bin Nasir and Arijit Raychowdhury, Madhavan Swaminathan, "Asynchronous Non-Linear Control of Digital Linear Voltage Regulator," US20210165437A1, 2020.

P27. Saad Bin Nasir and Arijit Raychowdhury, "Digital Low-Dropout Regulator (Régulateur numérique à faible relâchement)," WO-2019118745-A2 (EU patent), 2020.

D. Presentations

D1. IEEE Distinguished Lectures

1. "All-Digital and Digital-Assisted Integrated Low-Dropout Regulators (LDOs) for Fine-Grained Spatiotemporal Power Management of Digital Load Circuits" Switzerland (Zurich) IEEE SSCS Chapter, May 2021.
2. "All-Digital and Digital-Assisted Integrated Low-Dropout Regulators (LDOs) for Fine-Grained Spatiotemporal Power Management of Digital Load Circuits" Seattle IEEE SSCS Chapter, May 2021.
3. "Bits and Brains: Ultra-low Power, Neuro-inspired Edge-AI for Autonomous Systems" New Delhi (India) IEEE SSCS Chapter, India, June 2021.
4. "Bits and Brains: Ultra-low Power, Neuro-inspired Edge-AI for Autonomous Systems" Indonesia IEEE SSCS Chapter, Bali, Indonesia, July 2021.

D2. Selected Technical Panel Participation

1. "Memory Technologies on the horizon," Non-Volatile Memories Workshop, San Diego, March 2010.
2. "Non-volatile Memory for Embedded Systems: Is it worth the cost?" Non-Volatile Memories Workshop, San Diego, March 2011.
3. "Opportunities for Spintronics Memory," Non-Volatile Memories Workshop, Sendai, Japan, June 2012.
4. "Embedded Spin Based Memory Sub-systems," Spintronics Workshop, Honolulu, Hawaii, June 2012.
5. "Design Techniques for the IoT World," Custom Integrated Circuits Conference, San Jose, Sept 2015.
6. "Analog IP: Is there any scope in the fragmented and commoditized market?" Workshop on Test and Verification of High Speed Analog Circuits, Los Angeles, Oct. 2015.
7. "Fine-Grain Power Management" Design Automation Conference, June 2016.
8. "Innovative practices for variation-tolerant design of circuits/systems," VLSI Test Symposium, March, 2017.
9. "Transistor technology over the next ten years," Device Research Conference (DRC), South Bend, June 2017.
10. "Electronics Innovation's Great Leap Forward: An overview of the JUMP program" Design Automation Conference, June 2019.
11. "Foundry access for creating new technology demonstrators," NSF Workshop on Design of micro- and nano-electronic systems, Dec 2020.
12. "The future of design for AI," International Symposium on Electronics and Smart Devices (ISESD), June, 2021.

D3. Keynotes and Invited Seminar Presentations

1. "Designing with Subthreshold logic: From Devices to Systems," University of Florida, Gainesville, Florida, Mar. 2007.
2. "Subthreshold Design: Prospects and Challenges," University of Waterloo, Waterloo, Canada, Apr. 2007.
3. "Carbon Nanotube Electronics: Modeling, Circuit Implications, and Challenges," University of Michigan, Ann Arbor, May 2007.
4. "Designing Adaptive and Resilient Digital Systems," Invited Speaker Series, University of Washington, Washington, USA, Oct. 2010.
5. "Towards Resilient Circuits for Low Power Digital Microprocessors," Invited Speaker Series, Stanford University, Stanford, USA, Sept. 2011.
6. "High-Efficiency On-Die Digital Linear Voltage Regulators with On-Line Adaptation for Loads with Wide Dynamic Range of Operation," Qualcomm Inc., Raleigh, NC, USA, Oct. 2013.
7. "Linear Regulation: The Role of Adaptive Control," Intel Corporation, Hillsboro, OR, Nov. 2013.
8. "Voltage Regulators for Wide Dynamic Range," IBM T. J. Watson Research Lab, NY, Oct. 2014.
9. "Control Strategies for Linear Regulators in On-die Voltage Regulation of Digital Load Circuits," Qualcomm Research Lab, Raleigh, NC, Nov. 2015.
10. "Enabling Fine-grained Power Management through Distributed On-Die Voltage Regulators," Keysight Technologies Research Lab, San Jose, CA, Nov. 2015.
11. "Dynamical Systems and their Computing Properties," Invited Speaker Series, Stanford University, Stanford, USA, Dec. 2015.
12. "On-die Regulators for Fine-grained Power Management: Digital and Hybrid Topologies with Advanced Control Techniques," Intel Labs, Hillsboro, OR, May 2016.
13. "Computing with Dynamical Systems," IEEE Summer Topicals Meeting, Newport Beach, CA, July 2016.
14. "Advances in Digital and Mixed-Signal Circuits in Power Management, Sensing and Embedded Data Analytics," Qualcomm Research, Raleigh, NC, Dec 2016.
15. "Compressed Domain Classifiers on Mixed-Signal Hardware," Intel Corp, Hillsboro, OR, Dec 2016.
16. "Computing with Hardware based Dynamical Systems," Invited Speaker Series, Purdue University, West Lafayette, USA, March 2017.
17. "Advances in Linear Regulators: Design and Control," Qualcomm Inc, Raleigh, NC, June 2017.
18. "Advances in Linear Regulators: Design and Control," IBM T. J. Watson Research Lab, NY, Jan 2018.
19. "Embedded Linear Regulators," TSMC, Taiwan, Feb 2018.
20. "Edge Intelligence through Low-Power Circuits and Systems," ARM Ltd., Austin, Feb 2018.
21. "Dynamics of Coupled Oscillators for solving Hard Problems," DARPA Electronic Resurgence Initiative, Aug 2018.
22. "In-Memory Computing for Machine Learning Workloads," TSMC, Taiwan, Dec 2018.
23. "Beyond Vision Processing: Spiking Neural Networks for Optimizations and Control," SRC e-workshop, July 2019.

24. "Edge Intelligence for Sensing and Control," DARPA Electronic Resurgence Initiative, Detroit, Aug 2019.
25. "High-Efficiency System-on-Package High-Voltage Conversion for Power Delivery," SRC e-workshop, Nov 2019.
26. "Brain inspired Machines and Algorithms," Intel Corp., June, 2020.
27. "Near/In-Memory Computing for Data-Intensive Applications," DARPA Electronic Resurgence Initiative, Aug 2020.
28. "Enabling Secure Hardware through Embedded Sensors and Voltage Regulators," SRC e-workshop, November 2021.
29. "Composable Systems – How heterogeneous integration of logic and memory fabrics are accelerating memory-centric workloads," Information Systems and Computing Technology Network Symposium, Raytheon, May 2021.
30. "Accelerating ML workloads using Embedded In-RRAM-Computing," TSMC, June 2021.
31. "Merged logic and memory fabrics," Northrop Grumman University Symposium, 2021.

D4. Selected Tutorial Presentations

1. "Model study of 1T-1STT MTJ Memory Arrays for Embedded Applications," Midwest Symposium on Circuits and Systems (MWCAS), Aug. 2010.
2. "Design Considerations for 1T-1STT MTJ Based Embedded Memory Arrays," CSIS International Symposium on Spintronics Based VLSI, Sendai, Japan, Feb. 2011.
3. "1T-1STT MTJ Memory Arrays for Embedded Applications," Non-volatile Memory Workshop, San Diego, USA, March 2011.
4. "1T-1STT MTJ Based Embedded Memory Arrays," Spintronics Workshop on LSI, Hawaii, USA, Jun. 2012.
5. "Spintronics for Embedded Non-volatile Electronics," International Electron Device Meeting (IEDM), San Francisco, USA, Dec. 2012.
6. "Adaptive SRAM Circuits," Design and Test in Europe (DATE), Grenoble, France, Mar. 2013.
7. "Spintronics for Embedded Memory: A Model Study," International Symposium on Low Power Electronic Design, Oct. 2013.
8. "Computing with Spin: Beyond Charge Based Electronics," International Conference on Computer Aided Design (ICCAD), Nov. 2013.
9. "Adaptive and Resilient Circuits for Improving Energy Efficiency in Wide Dynamic Range Digital Systems," IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Monterey Bay, USA, Oct. 2013.
10. "On Die Digital Voltage Regulators with Continuous Time and Discrete Time Control for Loads with Wide Dynamic Range of Operation," IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), Austin, TX, May 2014.
11. "Adaptive Designs in Computation and Power Management," International Conference on Computer Aided Design (ICCAD), San Jose, CA, Nov. 2014.
12. "Integrated Power Management in IoT Devices under Wide Dynamic Ranges of Operation," Design Automation Conference (DAC), Austin, TX, June 2015.

13. "Digitizing On-die Regulators: A Scaling Perspective," International Symposium on Quality Electronic Design (ISQED), San Jose, CA, March 2016.

14. "Always ON Sensors for the Internet of Smart Things," Design Automation Conference (DAC), Austin, TX, June 2016.

15. "Fine-grained Power Delivery and Management in SoCs: Advances in Control and Circuit Design," IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), Honolulu, HI, Dec. 2016.

16. "Advances in Linear Regulators for Fine Grain Spatiotemporal Power Management in Digital Circuits," IEEE International Solid State Circuits Conference (ISSCC), San Francisco, CA, Feb. 2017.

17. "Embedded and Adaptive Voltage Regulators with Proactive Noise Reduction for Digital Loads Under Wide Dynamic Range," Texas Analog Center of Excellence (TxACE), University of Texas, Dallas, Apr. 2017.

18. "Computing with Dynamical Systems: Solving Optimizations and Inference Problems in Continuous Time," Semiconductor Research Corporation, Raleigh, NC, June 2017.

19. "EDA challenges in designing computing systems with post-CMOS devices," IEEE Conference on Rebooting Computing (ICRC). Washington, D.C., Nov. 2017.

20. "Tutorial: Emerging Computational Devices, Architectures and Computational Models," International Conference on VLSI Design, Pune, India, Jan. 2018.

21. "Energy-efficient Circuits and Systems for Emerging Neuro-inspired Computing," Workshop on Compound Semiconductor Materials and Devices (WOCSEMMAD), Feb 2018.

22. "Dynamics of Coupled Systems and their Computing Properties," IEEE International New Circuits and Systems Conference (NEWCAS), Montreal, Canada, Jun. 2018.

23. "Electromagnetic and Machine Learning Side-Channel Attacks and Low-overhead Generic Countermeasures," Conference on Cryptographic Hardware and Embedded Systems, Aug. 2019.

24. "Towards Memory-Centric Autonomous Systems: A Technology and Device Perspective," International Electron Device Meeting (IEDM), San Francisco, CA, Dec. 2019.

25. "TinyML: Ultra-Low Power Edge AI for Autonomous Systems," IEEE International Solid State Circuits Conference (ISSCC), San Francisco, CA, Feb. 2020.

26. "Electromagnetic and Machine Learning Side-Channel Attacks and Low-overhead Generic Countermeasures," International Symposium on Hardware Oriented Security and Trust (HOST), Dec. 2020.

27. "Merged Logic and Memory Fabrics for AI Workloads," Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 2021.

E. Grants and Contracts

E1. As Principal Investigator

1. **Title: Attack-resistant Voltage and Clocking Infrastructure for SoCs**
   Agency/Company: TSMC Center for Secure Microelectronics Ecosystem
   Amount: *USD 800,000*
   Role: *PI*
   Collaborator(s): None
   Period of Contract: *10/01/2021-09/30/2026*
   Candidate's Share: *100% (USD 800,000)*

2. **Title: High Voltage Point of Load Converters for Server Applications**
   Agency/Company: Intel
   Amount: *USD 300,000*
   Role: *PI*
   Collaborator(s): None
   Period of Contract: *03/01/2021-02/28/2024*
   Candidate's Share: *100% (USD 300,000)*

3. **Title: Computing by Merged Memory and Logic Fabric for Online Reinforcement Learning Algorithms using Ferroelectric Transistors**
   Agency/Company: DARPA
   Amount: *USD 250,000*
   Role: *PI*
   Collaborator(s): None
   Period of Contract: *01/01/2021-12/31/2021*
   Candidate's Share: *100% (USD 250,000)*

4. **Title: SCALE: Workforce Development Program**
   Agency/Company: DOD
   Amount: *USD 875,000*
   Role: *PI*
   Collaborator(s): None
   Period of Contract: *01/01/2021-12/31/2026*
   Candidate's Share: *100% (USD 8750,000)*

5. **Title: Cryogenically cooled CMOS for High Performance Computing**
   Agency/Company: Samsung GRO
   Amount: *USD 150,000*
   Role: *PI*
   Collaborator(s): None
   Period of Contract: *01/01/2021-12/31/2021*
   Candidate's Share: *100% (USD 150,000)*

6. **Title: Cryogenically cooled DRAM Design**
   Agency/Company: National Security Agency (NSA)
   Amount: *USD 100,000*
   Role: *PI*
   Collaborator(s): None
   Period of Contract: *08/01/2020-05/15/2021*
   Candidate's Share: *100% (USD 100,000)*

7. **Title: CCRI: Planning: Enabling Quantum Computer Science and Engineering Project Summary**
   Agency/Company: National Science Foundation (NSF)
   Amount: *USD 100,000*
   Role: *PI*
   Collaborator(s): None
   Period of Contract: *08/01/2020-07/31/2021*
   Candidate's Share: *100% (USD 100,000)*

8. **Title: EXPERT: EXPlainable-AI through Efficient Hardware-design in EmeRging Technologies**
   Agency/Company: Semiconductor Research Corporation
   Amount: *USD 375,000*
   Role: *PI*

Collaborator(s): None
Period of Contract: *01/01/2020-12/31/2022*
Candidate's Share: *50% (USD 187,500)*

9. **Title: EAGER: Collaborative: Machine-Learning based Side-Channel Attack and Hardware Countermeasures**
Agency/Company: National Science Foundation
Amount: *USD 300,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *07/01/2019-06/30/2021*
Candidate's Share: *50% (USD 150,000)*

10. **Title: Hierarchical Memory Systems to Enable Transfer Learning in Real-time Systems**
Agency/Company: Samsung
Amount: *USD 70,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *02/01/2019-01/31/2020*
Candidate's Share: *100% (USD 70,000)*

11. **Title: Emerging Algorithms and Computing Models for Cognition and Control on post-CMOS Hardware Platforms**
Agency/Company: Semiconductor Research Corporation
Amount: *USD 540,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *07/01/2018-12/31/2022*
Candidate's Share: *100% (USD 540,000)*

12. **Title: Machine Learning for Trusted Platform Design**
Agency/Company: Center for Advanced Electronics through Machine Learning
Amount: *USD 107,000*
Role: *PI*
Collaborator(s): Madhavan Swaminathan
Period of Contract: *01/01/2018-12/31/2019*
Candidate's Share: *50% (USD 53,500)*

13. **Title: JUMP: ASCENT: Applications and Systems driven Center for Energy-Efficient Integrated NanoTechnologies (ASCENT)**
Agency/Company: SRC and DARPA
Amount: *USD 3,380,361 (GT Amount) out of a total center funding of USD 29M)*
Role: *PI from GT (Center Director: Prof. Suman Datta, University of Notre Dame)*
Collaborator(s): Madhavan Swaminathan
Period of Contract: *01/01/2018-12/31/2022*
Candidate's Share: *52% (USD 1,752.680)*

14. **Title: JUMP: C-BRIC: Center for Brain-Inspired Computing Enabling Autonomous Intelligence (CBRIC)**
Agency/Company: SRC and DARPA
Amount: *USD 3,245,064 (GT Amount) out of a total center funding of USD 27M)*
Role: *PI from GT (Center Director: Kaushik Roy, Purdue University)*
Collaborator(s): Justin Romberg
Period of Contract: *01/01/2018-12/31/2022*
Candidate's Share: *50% (USD 1,622,532)*

15. **Title: EM and Power Side-Channel Attack Immunity through High-Efficiency Hardware Obfuscations**
Agency/Company: National Science Foundation
Amount: *USD 500,000*
Role: *PI*
Collaborator(s): Shreyas Sen
Period of Contract: *08/01/2017-03/31/2020*
Candidate's Share: *50% (USD 250,000)*

16. **Title: Ultra-Low Power Time-Domain (TD) Mixed-Signal (MS) Neural Network (NN) Hardware using All-Digital, Synthesizable Circuits**
Agency/Company: Qualcomm Inc.
Amount: *USD 70,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *04/01/2016-03/31/2017*
Candidate's Share: *100%*

17. **Title: Self-Powered IoT Sensor Node with In-situ Data Analytics and Energy-Aware End-to-end Real-time Optimization**
Agency/Company: SRC
Amount: *USD 425,124*
Role: *PI*
Collaborator(s): S. Sen (Purdue Univ)
Period of Contract: *12/01/2017-11/30/2020*
Candidate's Share: *63% (USD 264,624)*

18. **Title: E2CDA: Extremely Energy Efficient Collective Electronics (EXCEL)**
Agency/Company: NSF: 60% and SRC: 40%
Amount: *USD 4,419,225*
Role: *Center Co-Director and Theme Leader (Circuit Technologies)*
Collaborator(s): Twelve faculty members from GT, Univ of ND, Penn State, UCI
Period of Contract: *10/01/2017-09/30/2020*
Candidate's Share: *11% (USD 480,000)*

19. **Title: Unification of Voltage Regulation and High Performance Clocking Circuits**
Agency/Company: Qualcomm Inc.
Amount: *USD 70,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *07/01/2016-06/31/2017*
Candidate's Share: *100%*

20. **Title: Architecting STT-RAM to Address and Exploit Variability**
Agency/Company: Samsung Semiconductor USA
Amount: *USD 150,000*
Role: *PI*
Collaborator(s): Moinuddin Qureshi
Period of Contract: *07/15/2016-07/14/2018*
Candidate's Share: *50%*

21. **Title: Early Career Faculty Award**
Agency/Company: Intel Corporation
Amount: *USD 25,000*

Role: *PI*
Collaborator(s): None
Period of Contract: *No limit*
Candidate's Share: *100%*

22. **Title: Switched Mode Control and Load Balancing in Distributed Linear Regulators for Fine-Grained Spatiotemporal Power Management**
Agency/Company: Keysight Technologies
Amount: *USD 30,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *Jan. 2016 - Dec. 2016*
Candidate's Share: *100%*

23. **Title: CRII: SHF: Real-time Approximate-Dynamic-Programming based Neuro-controllers for Dynamic Power Management in Power-Constrained Digital Systems**
Agency/Company: National Science Foundation
Amount: *USD 254,000 (includes GT cost share)*
Role: *PI*
Collaborator(s): None
Period of Contract: *September 2015 - August 2017*
Candidate's Share: *100%*

24. **Title: Models, Algorithms and BIST Hardware Development for Manufacturing & Characterization Tests of Spin-Transfer-Torque MRAM Arrays**
Agency/Company: Semiconductor Research Corporation
Amount: *USD 195,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *December 2013 - November 2016*
Candidate's Share: *100%*

25. **Title: Embedded & Adaptive Voltage Regulators with Proactive Noise Reduction for Digital Loads under Wide Dynamic Range**
Agency/Company: Semiconductor Research Corporation
Amount: *USD 255,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *February 2014 - January 2017*
Candidate's Share: *100%*

26. **Title: Next Generation Power Management with Embedded All-Digital Voltage Regulators**
Agency/Company: Intel Corporation
Amount: *USD 360,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *December 2014 - November 2017*
Candidate's Share: *100%*

27. **Title: Hybrid Analog and Digital LDO VR for Fast Transient Response and High Steady-State Current Efficiency Project**
Agency/Company: Qualcomm Inc.
Amount: *USD 70,000*
Role: *PI*

Collaborator(s): None
Period of Contract: *May 2015 - April 2016*
Candidate's Share: *100%*

28. **Title: On-Die Load-Adaptive Voltage Regulator (VR) for Energy-Efficient Processor Design**
Agency/Company: Qualcomm Inc.
Amount: *USD 60,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *March 2014 - April 2015*
Candidate's Share: *100%*

29. **Title: Gesture Based Wakeup in an Always-On & Always-Connected Camera System using Algorithm-Hardware Co-Design in the Compressed Domain**
Agency/Company: Intel Corporation
Amount: *USD 240,000*
Role: *PI*
Collaborator(s): Justin Romberg
Period of Contract: *August 2014 - July 2017*
Candidate's Share: *50% (USD 120,000)*

30. **Title: Design and Analysis of Digital Low-Dropout Regulators for Fine-Grained and Embedded Power Management**
Agency/Company: Intel Corporation
Amount: *USD 70,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *June 2013 - May 2014*
Candidate's Share: *100%*

31. **Title: Algorithms and Hardware for Matching and Recognition**
Agency/Company: Intel Corporation
Amount: *USD 75,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *March 2013 - April 2014*
Candidate's Share: *100%*

32. **Title: Low-power FPGA Implementation of Boltzman Machines**
Agency/Company: Xilinx Corporation
Amount: *In Kind Gift priced at USD 4,500*
Role: *PI*
Collaborator(s): None
Period of Contract: *July 2013*
Candidate's Share: *100%*

E2. As Co-Principal Investigator

1. **Title: Elements:Open-source hardware and software evaluation system for UAV**
Agency/Company: National Science Foundation
Amount: *USD 600,000*
Role: *co-PI*
PI(s): Hyesoon Kim
Other Collaborator(s):

Period of Contract: *June 2021-May 2024*
Candidate's Share: *50% (USD 300,000)*

2. **Title: MURI: Cross-disciplinary Electronic-ionic Research Enabling Biologically Realistic Autonomous Learning (CEREBRAL)**
Agency/Company: AFOSR
Amount: *USD 7,124,304*
Role: *co-PI*
PI(s): Alan Doolittle
Other Collaborator(s): Eric Vogel, Louis Piper, Samuel Graham, Wei Cheng Lee
Period of Contract: *Aug. 2017-Jul. 2022*
Candidate's Share: *11% (USD 773, 286)*

3. **Title: Integrated Voltage Regulators for On-die Power Management**
Agency/Company: Power Delivery in Electronic Systems (PDES) - an Industry Consortium
Amount: *USD 840,000*
Role: *co-PI*
PI(s): Madhavan Swaminathan
Other Collaborator(s): S. Mukhopadhyay, H. Wang, P. Kohl
Period of Contract: *Oct. 2015-Sept. 2017 (Phase-I)*
Candidate's Share: *14% (USD 120,000) including fabrication cost*

F. Other Scholarly and Creative Accomplishments

1. Member, *EDN/EETimes's Editorial Advisory Board*, 2019 - present.

G. Societal and Policy Impacts

1. Dr. Raychowdhury, his students and collaborators demonstrated a breakthrough DRAM technology that can be integrated in a low-temperature back-end-of-line (BEOL) process with ability to accelerate AI workloads by two orders of magnitude. This was presented at the International Electron Device Meeting, Dec 2020 and covered by technology press, including IEEE Spectrum. [Link from IEEE Spectrum]

2. Dr. Raychowdhury and his group designed and demonstrated an ultra-low power mixed-signal chip inspired by the brain that provides palm-sized robots the ability to collaborate and learn from their experiences. Combined with new generations of low-power motors and sensors, the new application-specific integrated circuit (ASIC) – which operates on milliwatts of power – can help intelligent swarm robots operate for hours instead of minutes. This work was published at the International Solid Sate Circuits Conference in Feb, 2019 and was extensively covered by the media. [Link from Georgia Tech News] [Link from EETimes]

3. Dr. Raychowdhury, and his students developed the world's first scalable, many-core, fully-programmable optimization chip capable of solving a wide array of problems related to signal-processing, data-sciences and machine-learning. This was presented at the Custom Integrated Circuits Conference, 2019 and was covered by the popular media. This paved the way for similar research and several similar demonstrations from other industrial and academic research groups, and was popular media. [Link from IEEE Spectrum]

4. Dr. Raychowdhury and his students demonstrated the world's first hardware integrated circuit enabling reinforcement learning on edge devices in Feb 2018. This work was presented at the prestigious International Solid State Circuits Conference and covered by popular technology press. [Link from Electronics Weekly]

5. Dr. Raychowdhury and his research group in collaboration with researchers from the University of Notre Dame demonstrated through theory and experiments how a system of coupled dynamical oscillators can

synchronize to compute problems on representative graphs. In particular, they showed that synchronized oscillations can color binary graphs, a quintessential yet computationally hard problem in graph theory. This has far-reaching implications on analog computing primitives and was the resultant paper published in Nature Scientific Reports is the first article to establish the relationship between dynamical systems and algebraic graph theory. This work was covered by the technical media including the *R&D Magazine, Science Daily, Phys.org*. [Link from Georgia Tech News]

6. Dr. Raychowdhury's research group and his collaborators demonstrated the first smart camera capable of running completely on harvested energy in Feb, 2016. Apart from multiple technical publications, this work was widely covered by the press and appeared in *Wired, TechCrunch, NSF-News* among others. [Link from Georgia Tech ECE's Webpage]

7. Dr. Raychowdhury's research group and his collaborators demonstrated coherent coupling in phase transition oxide based oscillators and showed biomimetic properties of such networks. This work was published in Nature SR and was widely covered in *CNN, TechCrunch, NSF-News* and others. [Link from Penn State's Webpage]

8. Dr. Raychowdhury has contributed to the International Technology Roadmap for Semiconductors (ITRS) from 2011-2013 and to the International Roadmap for Device to Systems (IRDS) from 2017-present. ITRS and currently IRDS are the international consortia of semiconductor companies and academic researchers chartered to provide a roadmap of technology and technology-driven systems.

V. Education

A. Courses Taught

Semester/Year	Course Number	Course Title	Enrollment	CIOS Score
Spring 2013	ECE4130A	Advanced VLSI Systems	11	4.00
Spring 2013	ECE6130A	Advanced VLSI Systems	52	4.77
Summer 2013	ECE 2020A	Fundamentals of Digital System Design	35	4.00
Fall 2013	ECE 2020A	Fundamentals of Digital System Design	48	4.07
Spring 2014	ECE8893	Digital Design using Modern VLSI Devices	34	4.80
Summer 2014	ECE 2020A	Fundamentals of Digital System Design	36	4.30
Fall 2014	ECE4130A	Advanced VLSI Systems	17	4.10
Fall 2014	ECE6130A	Advanced VLSI Systems	92	4.70
Spring 2015	ECE4130A	Advanced VLSI Systems	5	NR
Spring 2015	ECE6130A	Advanced VLSI Systems	51	4.30
Summer 2015	ECE 2020A	Fundamentals of Digital System Design	36	4.50
Fall 2015	ECE8893	Digital Design using Modern VLSI Devices	15	5.00
Fall 2015	ECE 2020A	Fundamentals of Digital System Design	52	4.85
Spring 2016	ECE4130A	Advanced VLSI Systems	5	4.25
Spring 2016	ECE6130A	Advanced VLSI Systems	11	4.77
Summer 2016	ECE3030	Physical Foundations of Computing	25	4.78
Fall 2016	ECE2020A	Fundamentals of Digital System Design	50	4.72
Fall 2016	ECE2020B	Fundamentals of Digital System Design	45	4.74

Semester/Year	Course Number	Course Title	Enrollment	CIOS Score
Summer 2017	ECE 2020A	Fundamentals of Digital System Design	45	4.43
Fall 2017	ECE4130A	Advanced VLSI Systems	23	4.60
Fall 2017	ECE6130A	Advanced VLSI Systems	60	4.70
Spring 2018	ECE2020A	Fundamentals of Digital System Design	50	4.34
Spring 2018	ECE8193	Digital Design using Modern VLSI Devices	45	4.90
Summer 2018	ECE 2020B	Fundamentals of Digital System Design	50	4.40
Fall 2018	ECE4130A	Advanced VLSI Systems	23	4.80
Fall 2018	ECE6130A	Advanced VLSI Systems	60	4.80
Spring 2019	ECE 2020A	Fundamentals of Digital System Design	50	4.40
Spring 2019	ECE 2020B	Fundamentals of Digital System Design	50	4.20
Summer 2019	ECE 2020A	Fundamentals of Digital System Design	37	4.40
Fall 2019	ECE4130A	Advanced VLSI Systems	12	4.60
Fall 2019	ECE6130A	Advanced VLSI Systems	72	4.70
Spring 2020	ECE 2020A	Fundamentals of Digital System Design	50	NR

NR = Not Reported

B. Individual Student Guidance

B1. Ph.D. Students

B1.a. Ph.D. Students (Graduated)

1. Samantak Gangopadhyay
   Graduation Date: Dec, 2017
   Thesis Title: On-Die adaptive Power regulation and distribution for digital loads
   First Employment: AMD (Analog Research and Design Group)

2. Saad Bin Nasir
   Graduation Date: Dec, 2017
   Thesis Title: Fine-grain On-chip Power Management using Digital and Digitally-assisted Linear Voltage Regulators
   First Employment: Qualcomm Inc. (Power Management IC Research)

3. Anvesha Amaravati Graduation Date: Dec, 2018
   Thesis Title: Energy-efficienct Mixed-Signal Designs to Enable Edge AI
   First Employment: Qualcomm Corporate Research Division

4. Insik Yoon Graduation Date: Aug, 2019
   Thesis Title: Advanced memory Technologies for Autonomous System Design
   First Employment: Microsoft Research

5. Abhinav Parihar Graduation Date: Dec, 2019
   Thesis Title: Utilizing switched linear dynamics of interconnected state transition devices for approximating certain global functions

First Employment: Post-doc (Columbia U)

6. Ningyuan Cao Graduation Date: Aug, 2020
   Thesis Title: Circuit and algorithm design to enable edge intelligence
   First Employment: Assistant Professor (University of Notre Dame)

7. Muya Chang Graduation Date: Dec, 2020
   Thesis Title: Hardware Dynamical System for Solving Optimization Problems
   First Employment: Post-doc (Georgia Tech)

8. Aqeel Anwar Malik Graduation Date: May, 2021
   Thesis Title: Enabling Edge-Intelligence in Resource-Constrained Autonomous Systems
   First Employment: NVIDIA (Autonomous Vehicles)

B1.b. Ph.D. Students (In Process)

1. Bitan Bhar, PhD Student, ECE
   Fall 2017 to present
   Topic: Novel Computing Systems

2. Brian Crafton, PhD Student, ECE
   Fall 2018 to present
   Topic: Machine Learning Enabled through Hardware Design

3. Foroozan Karimzadeh, PhD Student, ECE
   Fall 2018 to present
   Topic: Hardware-driven Sparsification Techniques

4. Anupam Golder, PhD Student, ECE
   Fall 2018 to present
   Topic: Homomorphic Encryption Hardware and Design

5. Rakshith Saligram, PhD Student, ECE
   Spring 2019 to present
   Topic: Cryogenic CMOS Circuits and Design

6. Samuel Spetalnick, PhD Student, ECE
   Fall 2019 to present
   Topic: Non-volatile Memory Technologies

7. Ashwin Lele, PhD Student, ECE
   Fall 2019 to present
   Topic: Spiking Neural Networks in Perception and Control

8. Sitong Wu, PhD Student, ECE
   Fall 2019 to present
   Topic: High Voltage Converter Circuits

9. Minxiang Gong, PhD Student, ECE
   Fall 2019 to present
   Topic: GaN Based 48:1 V Converter Circuits

10. Ashwin Bhat, PhD Student, ECE
    Fall 2020 to present
    Topic: Hardware Primitives for XAI Systems

11. Nealson Li, PhD Student, ECE
    Fall 2020 to present
    Topic: Compute-Communicate Co-design for Wearables

12. Zishen Wan, PhD Student, ECE
    Fall 2020 to present
    Topic: SoC Architectures and Designs for Autonomous Navigation

13. Adou Sangbone Assoa, PhD Student, ECE
    Fall 2020 to present
    Topic: Physical Annealing Machines and Their Abilities to Solve Hard Problems

14. Jeongseok Lee, PhD Student, ECE (co-advised with Hua Wang)
    Fall 2019 to present
    Topic: RF digital transmitter and receiver frontends for sub-6GHz 5G wireless communication

B2. M.S. Students

B2.a. M.S. Students (In Process)

None

B2.b. M.S. Students (Graduated with Thesis)

1. Soundarya Bhagi, M.S. Student with Thesis, ECE (co-advised with Eric Vogel)
   Spring 2018 to Spring 2019
   Topic: Resistive Crossbar for Neural Network Sysnthesis
   First Employment: Intel Corporation, OR

2. Keval Kamdar, M.S. Student with Thesis, ECE
   Fall 2017 to Spring 2019
   Topic: Performance Estimation of Large Area Nanowires
   First Employment: Intel Corporation, OR

3. Ashwin Chintaluri, M.S. Student with Thesis, ECE
   Fall 2014 to Spring 2016
   Topic: Analysis of Defects and Fault Models in Embedded STT-MRAM Arrays
   First Employment: Microsoft Corporation, WA

4. Ashwin Subramanium, M.S. Student with Thesis, ECE
   Fall 2014 to Fall 2015
   Topic: Resilient Digital Circuits with Efficient Clock-Data Compensation
   First Employment: Apple Corporation, CA

5. Soham Desai, M.S. Student with Thesis, ECE
   Fall 2013 to Spring 2015 (Graduation)
   Topic: Hardware Implementation of Reconfigurable Restricted Boltzmann Machines for Image Recognition
   First Employment: Intel Labs, OR

B2.c. M.S. Students (Graduated non-Thesis)

1. Shipra Sharan, M.S. Student, ECE
   Spring 2016 to Fall 2017
   Topic: FPGA Implementation of RISC Rocket Core with Fine-grain Power Management
   First Employment: Microsoft, Raleigh

2. Zhilun Li, M.S. Student, ECE
   Spring 2013 to Spring 2014
   Topic: Energy-Accuracy Trade-offs in Compressive Sensing Cameras
   First Employment: Oracle, CA

3. Youngtak Lee, M.S. Student, ECE
   Spring 2013 to Fall 2014
   Topic: Low Drop-out Digital Regulators
   First Employment: PreScouter Inc., GA

4. Anirudha Kurkhade, M.S. Student with Thesis, ECE
   Spring 2015 to Fall 2016
   Topic: Phase Transition Materials in Spiking Neural Circuits

B3.a. Undergraduate Students (In Process)

1. Johnathan Law, B.S. Student, ECE
   Start Date: Spring, 2020
   Research Topic: Hardware for AI

2. Ananth Kumar, B.S. Student, ECE
   Start Date: Summer, 2020
   Research Topic: Software-hardware co-design for TinyML

3. Lindsey Lubin, B.S. Student, ECE
   Start Date: Summer, 2021
   Research Topic: Brain-inspired dynamics cognition and control

4. Connor Talley, B.S. Student, ECE
   Start Date: Spring, 2021
   Research Topic: Circuit and system design with embedded resisitive RAM

B3.b. Undergraduate Students (Graduated)

1. Justin Ting, B.S. Student, ECE
   Spring, 2016 - Spring, 2021
   Topic: Hardware Support for Reinforcement Learning for Mobile Robotics

2. Sitong Wu, B.S. Student, ECE
   Summer, Fall 2015
   Topic: ASIC support for deep learning

3. Chirag Medpara, B.S. Student, ECE
   Spring 2016
   Topic: ASIC support for deep learning

4. Soham Roy, B.Tech. Student, EE, Indian Institute of Tech, Delhi
   Summer 2016
   Topic: Switched Mode Fast Locking Phase Locked Loops

B4. Service on Thesis or Dissertation Committees

B4.a. Internal (Georgia Tech)

Proposal and Defense Committees

Student	School	Date of Proposal Exam / Graduation
Kwanyeob Chae	School of ECE	Aug. 2013
Xian Wang	School of ECE	Dec. 2014
Shreepad Pant	School of ECE	Apr. 2015
Satyan Telikepalli	School of ECE	May 2015
Wen Yuen	School of ECE	Aug. 2015
Boris Alexandrov	School of ECE	Aug. 2015
Amit Trivedi	School of ECE	Sep. 2015
Taigon Song	School of ECE	Oct. 2015
Sergio Carlos	School of ECE	Oct. 2015
Jayaram Natarjan	School of ECE	May 2016
Khondker Zakir Ahmed	School of ECE	July 2016
Yang Zhang	School of ECE	Aug. 2017
Sourav Datta	School of ECE	Dec 2017
Thomas Sarvey	School of ECE	Jan. 2018
Kyungwook Chang	School of ECE	Sept. 2018
Bon Woong Ku	School of ECE	Dec. 2018
Huan Yu	School of ECE	Dec. 2018
Zaid Ebrahim	School of ECE	Aug. 2019
Yun Long	School of ECE	Aug. 2019
Shaojie Xu	School of ECE	March 2020

Student	School	Date of Proposal Exam / Graduation
Xiaoyu Sun	School of ECE	June 2020
Hakki Mert Torun	School of ECE	Sept. 2020
Zang Wang	School of ECE	Sept. 2020
Devon Janke	School of ECE	May 2021
Majid Ahadi Dolatsara	School of ECE	May 2021
Claudio ALvarez	School of ECE	June 2021

B4.b. External

Student	University	Advisor	Date of Graduation
Rangharajan Venkatesan	Purdue University	Prof. A. Raghunathan	Summer 2014
Sumeet K. Gupta	Purdue University	Prof. K. Roy	Summer 2012
Charles Augustine	Purdue University	Prof. K. Roy	Summer 2011
Fahim Ur Rahman	Univ. of Washington	Prof. V. Sathe	Spring 2018
Aditya Raj	Univ. of California Santa Barbara	Prof. U. Mishra	Fall 2020

B5. Mentorship of postdoctoral fellows or visiting scholars

1. Dr. Kaushik Bhattacharya
   Highest Degree: PhD (Indian Institute of Technology, Kharagpur, India)
   April 2018 to June 2019
   Research Topic: High-voltage Embedded Power Converters
   Employment: Assistant Professor (NIIT, India)

2. Dr. Jong-Hyeok Yoon
   Highest Degree: PhD (KAIST, Republic of Korea)
   Nov 2018 to April 2020
   Research Topic: Hardware design for Edge-AI
   Employment: Assistant Professor (Daegu Gyeongbuk Institute of Science and Technology (DGIST) , Republic of Korea)

3. Dr. Yan Fang
   Highest Degree: PhD (Univ of Pittsburg, USA)
   Oct 2018 to present
   Research Topic: Dynamical Systems and Computing Models
   Employment: Assistant Professor (Kennesaw State University, to start in spring 2021)

4. Dr. Ningyuan Cao
   Highest Degree: PhD (Georgia Tech, USA)
   Oct 2018 to present
   Research Topic: Ultra-low power Circuits for Edge-AI
   Employment: Assistant Professor (University of Notre Dame, to start in spring 2021)

5. Dr. Muya Chang
   Highest Degree: PhD (Georgia Tech, USA)
   Jan 2021 to present
   Research Topic: Hardware systems for Embedded Optimizations

6. Dr. Bidyut Bhattacharjee (Research Engineer)
   Highest Degree: PhD
   July 2021 to present
   Research Topic: SiP Modules for High Power Conversion and Delivery

7. Dr. Sigang Ryu
   Highest Degree: PhD (Seoul National University, Repblic of Korea)
   August 2021 to present
   Research Topic: Designing low-power systems in RRAM

C. Educational Innovations and Other Contributions

C1. Course Development

ECE8893 Digital Design using Modern VLSI Devices: This is a graduate-level course on the fundamentals of nano-scaled electron devices and their role in digital VLSI design. Dr. Raychowdhury developed this course to provide an overview of both the fundamentals of digital VLSI devices in terms of their electrostatic and transport properties, as well as to cover the state of the art design techniques that address some of the device level challenges. The course has assignments and a project. Students are taught how to think of MOSFETs intuitively and what the major device breakthroughs in the last ten technology nodes have been. In the second half of the course, the students are exposed to advanced VLSI design techniques that address critical challenges like increased transistor leakage and excessive device parameter variation, as well as design topologies that are resilient to variation and noise.

C2. Course Improvement

1. Dr. Raychowdhury with Prof. Sudhakar Yalamanchili to introduce the concepts of delay and energy dissipation in ECE 2020. This provides the students with foundational understanding of the different trade-offs in digital systems and what the growing challenges in digital design are.

2. Introduced the notion of energy efficient design in ECE6130/4130 through a revamped course design. Super-threshold, near-threshold and sub-threshold designs are now explored in details to meet the current demand of the industry.

C3. Educational Outreach

SCALE-SoC: Workforce Development for System-on-Chip Design: Prof Raychowdhury is the PI and the site Director for the DoD sponsored SCALE-SoC program. This is targeted towards undergraduate students who are US citizens. Students will be trained on the principles of SoC design with the objective to developing the talent pipeline for National Labs, defense industrial base and the Department of Defense.

VI. Service

A. Professional Contributions

A1. Editorial

Associate Editor	*IEEE Transactions on Computer Aided Design*, 2015 - 2019
Editor	*Microelectronics Journal*, 2014 - 2018
Guest Editor	*IEEE Design and Test Magazine*, Dec 2018
Special Issue Editor	*IEEE Design and Test Magazine*, Feb 2018

Guest Editor *ACM Journal on Emerging Technologies in Computing Systems: Special Issue on Emerging Memory Technologies*, May 2013

A2. Memberships and Activities in Professional Societies

1. Distinguished Lecturer, IEEE Solid State Circuits Society, 2021-2022
2. Mentor for Early-Career Engineers, IEEE Solid State Circuits Society, 2020-present
3. Panel Member and Member of Selection Committee for Senior Members, The Institute of Electrical and Electronics Engineers (IEEE) South-East Region, 2019-2021
4. Senior Member, The Institute of Electrical and Electronics Engineers (IEEE)
5. Member, The Association for Computing Machinery (ACM)

A3. Organization and Chairmanship of Technical Sessions, Workshops, and Conferences

1. **Steering Committee Member**, Custom Integrated Circuits Conference (CICC), 2021 - present
2. **Technical Program Chair**, Custom Integrated Circuits Conference (CICC), 2022
3. **Technical Program Co-Chair**, Custom Integrated Circuits Conference (CICC), 2021
4. **Technical Program Co-Chair**, Artificial Intelligence Circuits and Systems (AICAS), 2021
5. **Forum Organizer**, International Solid State Circuits Conference (ISSCC) 2020
6. **Track Chair**, Design Automation Conference (DAC) 2018, 2019, 2020, 2021
7. **Forum Chair**, Custom Integrated Circuits Conference (CICC) 2018, 2019
8. **Tutorial Chair**, International Symposium on Quality Electronic Design (ISQED) 2014, 2015
9. **Track Chair**, VLSI Conference 2014, 2015, 2016
10. **Track Chair**, International Conference on Computer Aided Design (ICCAD) 2010, 2011

Membership in Conference Technical Committee

1. International Solid State Circuits Conference (ISSCC), 2020 - present
2. VLSI Circuit Symposium (VLSIC), 2020 - present
3. Design Automation and Test in Europe (DATE) 2017 - present
4. Design Automation Conference (DAC) 2012-2015, 2018 - present
5. Custom Integrated Circuits Conference (CICC) 2015 - present
6. Workshop on Test & Verification of High Speed Analog Circuits (TVHSAC) 2015
7. International Symposium on Low Power Electronic Design (ISLPED) 2018, 2017, 2016, 2015, 2014, 2013
8. International Conference on Computer Aided Design (ICCAD) 2019, 2018, 2012, 2011, 2010, 2009, 2008
9. International Symposium on Quality Electronic Design (ISQED) 2017, 2016, 2015, 2014, 2013, 2012, 2011, 2010, 2009, 2008
10. VLSI Conference 2014, 2011, 2010

A4. Technical Journal and Conference Referee

1. *Nature Electronics*
2. *Nature Communications*
3. *IEEE Solid State Circuits Letters (SSC-L)*
4. *IEEE Journal of Solid State Circuits (JSSC)*
5. *IEEE Transactions on VLSI Systems (TVLSI)*
6. *IEEE Transactions on Electron Devices(TED)*
7. *IEEE Transactions on Circuits and Systems (TCAS) I & II*
8. *IEEE Transactions on Computer Aided Design (TCAD)*
9. *IEEE Transactions on Nanotechnology (TNANO)*
10. *Frontiers of Neuroscience*
11. *IEE Proceedings - Circuits, Devices and Systems*
12. *Microelectronics Journal*
13. International Symposium on Low Power Electronics and Design (ISLPED)
14. International Symposium on Quality Electronic Design (ISQED)
15. International Symposium on Circuits and Systems (ISCAS)
16. International SOC Design Conference (ISOCC)
17. Design Automation Conference (DAC)
18. Custom Integrated Circuits Conference (CICC)
19. International Conference on Computer Aided Design (ICCAD)

A5. Proposal Panel Reviews

1. Panelist, Pazy Foundation, Israel, May 2021
2. Panelist, National Science Foundation, ENG Directorate, Feb 2021
3. Panelist, National Science Foundation, CISE Directorate, Jan 2021
4. Panelist, National Science Foundation, CISE Directorate, Nov 2020
5. Panelist, National Science Foundation, ENG Directorate, June 2020
6. Panelist, National Science Foundation, CISE Directorate, Feb 2020
7. Panelist, National Science Foundation, CISE Directorate, May 2019
8. Panelist, National Science Foundation, CISE Directorate, Aug 2018
9. Panelist, National Science Foundation, CISE Directorate, Jan 2018
10. Panelist, National Science Foundation, CISE Directorate, Dec 2017
11. Panelist, National Science Foundation, CISE Directorate, April 2016

12. Panelist, National Science Foundation, CISE Directorate, Dec 2015
13. Panelist, National Science Foundation, CISE Directorate, Jan 2010
14. Reviewer & Panelist, Semiconductor Research Corporation (Global Research Council), 2011

A6. Standardization and Roadmap Committes

Technical Contributor	International Roadmap for Devices and Systems, 2017-2020 Editions
Technical Contributor	International Technology Roadmap for Semiconductors, 2010-2012 Editions

A7. Other Involvement

Industry Liaison	Emerging Technologies Theme, C2S2 Center, FCRP, 2008-2012
Industry Mentor	Several SRC Projects, Nano-electronics Research Initiative (NRI), 2010-2012

B. Public and Community Service

1. Initiated summer internship for high school students on selected topics in Computer Engineering, 2017 - 2019.
2. Hosted one high school teacher as a part of the RET (Research Experience for Teachers) program, in collaboration with Georgia Tech's Center for Education Integrating Science, Mathematics, and Computing (CEISMC), 2019.

C. Institute Contributions

C1. Institute Committee Service

1. Member, Search Committee for the Dean of the College of Engineering, 2020

C2. School Committee Service

1. Statutory Advisory Committee, 2020-present
2. Graduate Committee, 2020-present
3. Graduate Committee, 2019-2020
4. Graduate Committee, 2018-2019
5. Graduate Committee, 2017-2018
6. Graduate Committee, 2016-2017
7. Graduate Committee, 2015-2016
8. Graduate Committee, 2014-2015

C3. Program Development: Research

1. **Center for Circuits and Systems (CCS):** Dr. Raychowdhury is currently the Director for the Center for Circuits and Systems (CCS). He was instrumental in setting up the center with a charter to bring together researchers in circuit and system design with an emphasis on computation and technology-circuit interactions. CCS is also the home of IEEE Atlanta chapter's Solid State Circuits Society (SSCS) and Circuits and Systems (CAS) chapters.

2. **Georgia Tech Quantum Alliance (GTQA):** Dr. Raychowdhury is currently the Co-Director for the Georgia Tech Quantum Alliance (GTQA) which is a part of the Institute for Electronics and Nanotechnology. He played a key role in setting up the alliance, which brings together researchers from the colleges of science, engineering and computing to collaborate and innovate of various aspects of quantum computing and information processing. The alliance provides support to graduate students and provides a platform for collaborating on university-wide efforts such as proposal preparations and invited seminars.

3. **Center for Co-Design of Chips, Packaging and Systems (C3PS):** Dr. Raychowdhury was the Associate Director for the Center for Co-Design of Chips, Packaging and Systems which is a part of the Institute for Electronics and Nanotechnology from 2017 to 2019. He played a key role in setting up the industry consortium, namely Power Delivery in Electronic Systems (PDES) in 2016. The PDES consortium consists of broad thrust areas to address the power delivery challenges for integrated systems. It is currently supported by eight companies and funds collaborative research among six faculty members. PDES was subsequently merged with the Packaging Research Center.

4. **ASCENT: Applications and Systems driven Center for Energy-Efficient Integrated NanoTechnologies (ASCENT)** Dr. Raychowdhury led Georgia Tech's effort and collaborated with twenty researchers across the nation to establish the ASCENT center, which is led by the University of Notre Dame. This is a $30M center chartered by the Semiconductor Research Corporation and DARPA to investigate the next generation of platform technologies to enable break-through performance and energy-efficiency in computing platforms over the next five years (2018-2022). Dr. Raychowdhury leads the research theme of *Heterogeneous Integration*, one of the four themes in the center. The ASCENT center currently funds research efforts by Dr. Raychowdhury and Dr. Swaminathan from Georgia Tech.

5. **C-BRIC: Center for Brain-Inspired Computing Enabling Autonomous Intelligence** Dr. Raychowdhury led Georgia Tech's effort in establishing the C-BRIC center, which is led by Purdue University. This is a $27M center (2018-2022) chartered by the Semiconductor Research Corporation and DARPA to investigate the next-frontiers of Artificial Intelligence, both from algorithms and hardware perspectives. Dr. Raychowdhury leads the theme on *Neural Fabrics*, one of the four research themes in the center. The C-BRIC center currently funds research efforts by Dr. Raychowdhury and Dr. Romberg from Georgia Tech.

C4. Program Development: Academic

1. **SCALE SoC: Scalable Asymmetric Lifecycle Engagement** Dr. Raychowdhury is the Principle Investigator and Site Director for the nation-wide effort for workforce development in SoC design. Through this multi-year effort Georgia Tech will be partnering with Purdue, Ohio State and UC Berkeley to develop a SoC design curriculum, involvement of undergraduate students in research, placement of students for internships in govt. labs and overall workforce development for the Department of Defense.

C5. Other Institute Service and Program Participation

1. **Provost's Emerging Leaders Program:** Dr. Raychowdhury was a member of the 2019-2020 cohort of the Provost's Emerging Leaders Program. The program, which is a collaboration among the Office of the Provost, the Office of the Executive Vice President for Research, the Institute for Leadership and

Social Impact, and the Office of Graduate Education and Faculty Development, is designed to provide participants with an overview of the leadership challenges and opportunities at Georgia Tech.