Scaled Back End of Line Interconnects at Cryogenic Temperatures

Rakshith Saligram, Suman Datta, Arijit Raychowdhury

***Abstract*— At scaled nodes, Back End of Line (BEOL) interconnect resistance increases super-linearly and creates performance and energy bottlenecks. While it is known that metal resistance deceases with temperature, understanding and quantifying the behavior of interconnects from a foundry process design kit (PDK) at low temperature is critical for designing circuits and systems operating at cryogenic temperatures including Quantum and Superconducting Computers and other High-Performance Systems. In this paper we use parametric path based ring oscillators along with reference ring oscillators and Metal-on-Metal Capacitors for 22nm Fully Depleted Silicon on Insulator to measure RC delays of BEOL elements from room temperature to 4.2K. The extracted resistance of the elements show reduction of up to 30% for M1/M2, 33% for M3-M6 and 19% for Via1. With simple assumptions for interconnect structure, we perform least-squares fit of Fuchs-Sondheimer-Mayadas-Shatzkes (FS-MS) models with line-Edge roughness incorporated in the model using the Namba Model. The empirically fitted parameters track well with literature. The fitted model is within 3.7% error of all experimental results.**

***Index Terms*—BEOL Interconnects, Current Starved Ring Oscillators, Cryogenic Temperatures, Fuchs-Sondheimer-Mayadas-Shatzkes Models, RC Delay, Resistivity**

I. Introduction

BACK End of Line (BEOL) interconnects often contribute to the critical paths of digital designs creating performance bottlenecks in scaled nodes [1]. Fig. 1 shows the Elmore delay breakdown of top critical paths in High Performance CPU across foundry nodes [2]. As the BEOL interconnect geometries shrink, other challenges such as electromigration (EM) start to show up, further deteriorating the performance (partly mitigated by subtractive reactive ion etch [3]). One of the benefits of operating CMOS at cryogenic temperatures is reduced interconnect resistance. It has been well studied and understood that copper interconnects scale well with temperature [4][5], however these studies have not yet been conducted on scaled commercially available process technologies. In this paper, we use test structures including capacitively loaded parametric ring oscillator structures fabricated on a 22nm Fully-Depleted Silicon on Insulator (FDSOI) process to estimate the delay of interconnects and then evaluate the resistance of different metal layers (M1-M6) from 300K to 4.2K.

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We further calculate the resistivity and explain the observations using a calibrated Fuchs-Sondheimer and Mayadas-Shatzkes (FS-MS) [6-9] model while accounting for Line Edge Roughness (LER) from the Namba model [10]. The rest of the paper is organized as follows: in section II, we explain the design and test structures; in section III we analyze the results, explain the assumptions of the model, and analyze the fitted model.

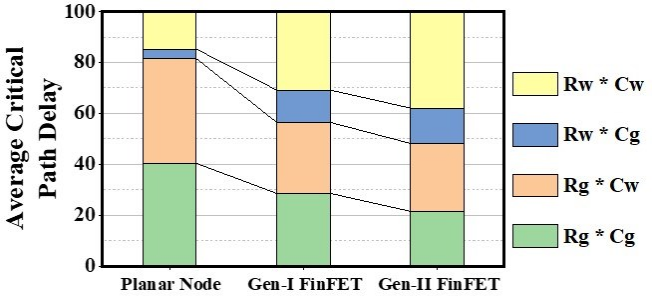


Fig. 1. Elmore Delay Breakdown of top critical paths in High Performance CPU across foundry nodes. Rw, Cw: Wire Resistance & Capacitance, Rg, Cg: Gate Resistance & Capacitance

II. Parametric Ring Oscillators

Ring Oscillators (ROs) have typically been used to characterize standard cell delays, monitor process variations [11, 12] and perform path delay measurements [13][14]. ROs generally comprise of an odd number of single ended inverting stages connected in a feedback loop and the propagation delay of the signal through the stages determines the period of oscillation. The period/frequency can be controlled by controlling the delay though each stage and one way to control the delay is to control the amount of current available to charge/discharge capacitive load of the stage (current starving). Current Starved Ring Voltage Controlled Oscillator (VCO) uses variable bias currents to control its oscillation frequency. Additional stage capacitors can be included to lower the frequency of oscillation to provide higher measurement resolution amidst phase noise and jitter.

The calibrating or reference baseline design is a 11 stage capacitively loaded current starved RO as shown in Fig. 2. The test structures for measuring interconnect performance consist of a parametric path based ring oscillator, same as the baseline with the exception of test elements placed in the feedback loop. Metal-on-Metal (MOM) capacitors are added at output of each stage to limit the oscillation frequency.

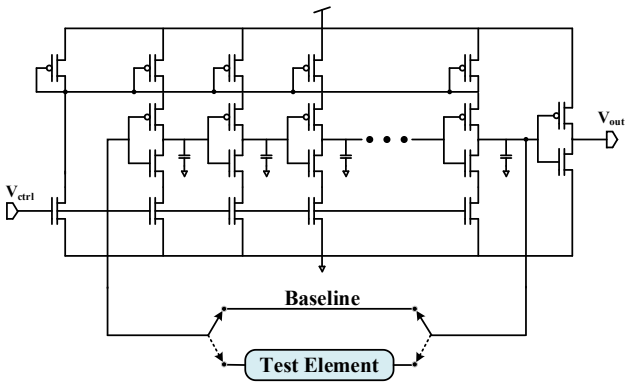


Fig. 2. Calibrating Baseline and Parametric Path Based capacitively loaded current starved RO

The different test structures are long lengths of snaked M1, M2, Mx (x=3-6) and M1-V1-M2. For the last structure, multiple vias are placed at minimum allowable distance across the entire length of M1-M2. The die photograph of 22nm FDSOI test chip with RO structures and MOM caps is shown in Fig. (3(a)). The MOM caps used in the design are tested separately to account for variability across temperature and calibrated out in the measurements. The delay of the test element is proportional to the difference in the time period of baseline (T_{base}) and the parametric path-based ring oscillators (T_{test}).

$$t_d \propto T_{test} - T_{base} \quad (1)$$

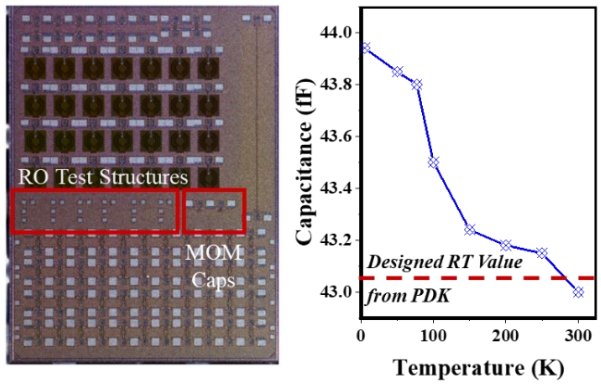
III. Measurement Results and Modelling

A. Results:

First, we measure the MOM capacitors across different temperatures at frequency of 1MHz with input RMS voltage of 30mV. To account for the pad capacitance, the probes are calibrated for open circuit and short circuit conditions at each temperature. The variation of the capacitance value (Fig. 3(b)) from room temperature to 4.2K is minimal (~2.2%) and is due to slight change in the dielectric constant [15].

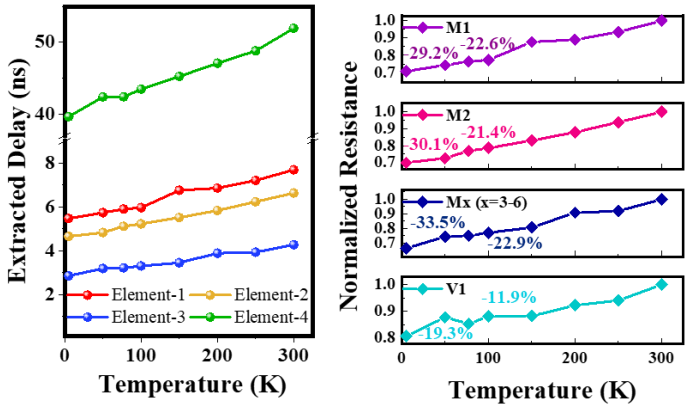
The frequency of oscillation is determined at multiple control voltages for the baseline and the test ROs across temperature. The stage delay of the baseline RO is computed, and the delay of the test element is extracted based on simple RC models calibrating out the variation in external MOM capacitance. The extracted delay for the four test elements is shown in Fig. 4(a). The value of the interconnect capacitance, which in itself is a small component of the overall capacitive load, is assumed to be constant across temperature.

Using the extracted RC delay and capacitance values, the resistance of the interconnects and via can be estimated. The variation of resistance for these layers across temperature is shown in Fig. 4(b). The data has been normalized to room temperature value and shows ~30% improvement for M1 and M2, ~33% for Mx (x=3-6) and ~19% for V1. The measured results track the process defined values at room temperature (Fig. 5(a)) shown as normalized values for M1, M2, Mx (x=3-6) (Ω/μm) and V1 (Ω/via) BEOL layers. The LL and UL denote the upper limit and lower limit specified in the PDK.



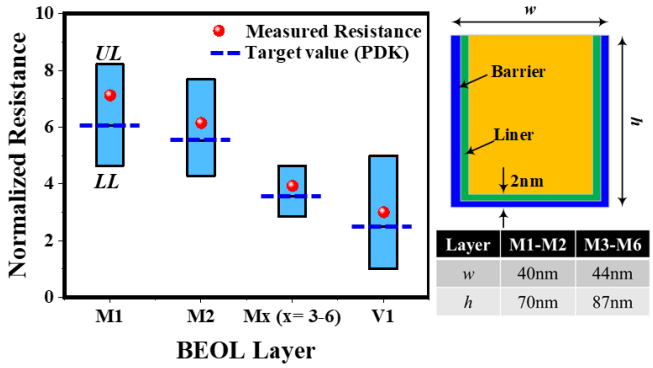
(a) (b)

Fig. 3. (a) 22nm FDSOI Chip Photograph showing ROs and MOM Caps (b) Measured MOM Cap across temperature.



(a) (b)

Fig. 4. (a) Extracted Delay from measured frequencies of baseline and parametric ROs across temperature (b) Extracted normalized resistances across temperature (% decrease shown for 100K & 4K).



(a) (b)

Fig. 5. (a) Measured Resistance of BEOL layers compared with PDK values at Room Temperature. (b) Model of interconnects

B. Modelling:

In prior work, interconnects have been modeled using semi-empirical methods at room temperature [16] [17]. In order to explain the measured results, we fit parameters from classic FS-MS models and account for LER contribution from Namba Model for the M1-M6 layers across the wide range of temperature from 4.2K to 300K.

1) Assumptions: The width and height of the interconnect are known from the PDK. We assume that the copper interconnect is encapsulated on the sides and the bottom by both barrier and liner materials with total thickness of $t_{bar/lin}$ (~2nm) on all sides and zero taper angle θ_{taper} (Fig. 5(b)). Typically, this material is TaN/Ta or TaN/Co but its exact composition is ignored as the resistance of the barrier/liner is very high, and the do not contribute to the effective resistance of the interconnect. Next, we assume that the distance between the grain boundaries is equal to the minimum feature dimension of the interconnect which will be 36nm (40nm) for M1-M2 (M3-M6). Finally, the 2nm barrier/liner assumption implies 68nm (85nm) Cu interconnect height for M1-M2 (M3-M6) respectively.

2) Model: The bulk resistivity of Cu is determined by (2) along with the Bloch-Gruneisen equation [5]

$$\rho_0(T) = A\left[1 + \frac{BT}{\theta - CT} + D\left(\frac{\theta - CT}{T}\right)^P\right]\varphi\left(\frac{\theta - CT}{T}\right) \quad (2)$$

$$\varphi(x) = 4x^{-5}\int_0^x z^5 e^z (e^z - 1)^{-2} dz \quad (3)$$

where A= 1.809 x10^{-9}Ωm, B= -6 x10^{-3}, C= 0.0456 x10^{-3}, D = -6.476 x10^{-4}, P = 1.84, θ= 310.8K are fitting parameters [5].

The closed form effective resistivity as a function of line edge roughness (LER), sidewall specularity p, grain boundary scattering reflection coefficient R, height of interconnect h, width of interconnect w and LER amplitude u is given by [14] although the assumption LER period being much greater than electron mean free path needs re-investigation at cryogenic temperatures.

$$\rho_{eff}(T) = \frac{\rho_0(T)}{\sqrt{1 - \left(\frac{u}{w}\right)^2}}\left[G(\alpha(T)) + 0.45\lambda(1-p)\left(\frac{1}{h} + \frac{1}{w\left[1 - \left(\frac{u}{w}\right)^2\right]}\right)\right] \quad (4)$$

where the grain boundary MS component G(α(T)) is defined as

$$G(\alpha) = \frac{1}{3}\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)\right] \quad (5)$$

$$\alpha(T) = \frac{\lambda(T)}{d}\frac{R}{1-R} \quad (6)$$

$\lambda(T)$ is determined by electron gas theory $\rho_0(T)\lambda(T) = 6.6\text{x}10^{-16}$.

3) Fitting: The bulk resistivity is determined from (2) and (3) by using accurate analytical representation for Bloch-Gruneisen from [19] and the electron mean free path is computed from the above relation. ρ_{eff} per unit length at a given temperature is calculated with ρ_{eff} = R.A where R is the measured resistance and A is the cross section area after accounting for barrier/liner thickness. With u, R and p as the fitting parameters, a least-mean-square fit is performed and the fitted parameters along with the model/experiment values is shown in Table 1. The LER amplitude, specularity parameters are within acceptable limits [18], however, two grain boundary reflection coefficients are used, one for temperature above 200K and other for below 200K to obtain close fit. The presence of two distinct reflection coefficients suggests either that the barrier potential of the grain boundary is different between RT and cryogenic temperature or that there are other temperature dependent scattering mechanisms at play [20].

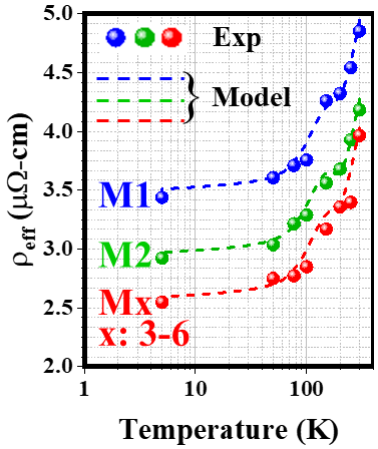


Fig. 6 Fitted Model versus experimental data for ρ_{eff} of various metal layers.

TABLE 1: PARAMETERS VALUES FOR FITTED CURVE

Parameter	Value	Source
d	36nm: M1-M2 40nm: M3-M6	Assumption
t_{liner}	2nm	Assumption
h	68nm: M1-M2 85nm: M3-M6	Assumption/PDK
w	36nm: M1-M2 40nm: M3-M6	Assumption/PDK
θ_{taper}	0^0	Assumption
u	10.95nm: M1-M2 12.5nm : M3-M6	Fitted
p	0.375: M1 0.450: M2-M6	Fitted
R	0.375-0.505	Fitted

IV. CONCLUSIONS

In this paper we report the BEOL interconnect delay at cryogenic temperatures for a full stack 22nm FDSOI foundry process which is, to the best of our knowledge, the first such effort in understanding the scaled RC time constants at low temperature. This knowledge of RC delay variation with temperature is vital and will assist in building better cryogenic high performance compute systems. We deploy a novel approach using parametric path based voltage controlled ring oscillators to accurately measure the delay and hence the resistance for multiple both local and intermediate metal layers (M1-M6) and also a via (V1). We then use the Fuchs-Sondheimer-Mayadas-Shatzkes (FS-MS) models along with the Namba Model for Line-Edge roughness, to evaluate the resistance scaling of the metal interconnect stack at cryogenic temperatures. Experimental results from a suite of test-structures in 22nm FDSOI provide good match with the proposed models.

ACKNOWLEDGEMENTS

We would like to thank Wriddhi Chakraborty, Khandker Akif Aabrar and Abhishek Khanna at University of Notre Dame for helping set up the measurements.

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