HW3 Solutions ECE2060 Sp 2022

Problems start from next page. 5 problems were graded, each graded problem is worth 2 points. Graded problems were: 1, 2, 3, 4 and 5

The problem numbers are from your text book (both the 6th and 7th edition will work)

1) Problem 9.4 a, b (do not use any NOT gates). Use the truth table shown on page 2 of Lesson 10 (on our website) for the full adder. This truth table also defines the meaning of the variables X, Y and Z. . Connect X, Y, Z inputs to the inputs a, b, c respectively of the decoder shown in Fig. 9-17 of the book.

Note1: Realizing a full adder means implementing a full adder.
Note2: Use X, Y, Z and connect them to a, b, c exactly as asked in this question. If you mix these variables up then answer will be considered wrong.

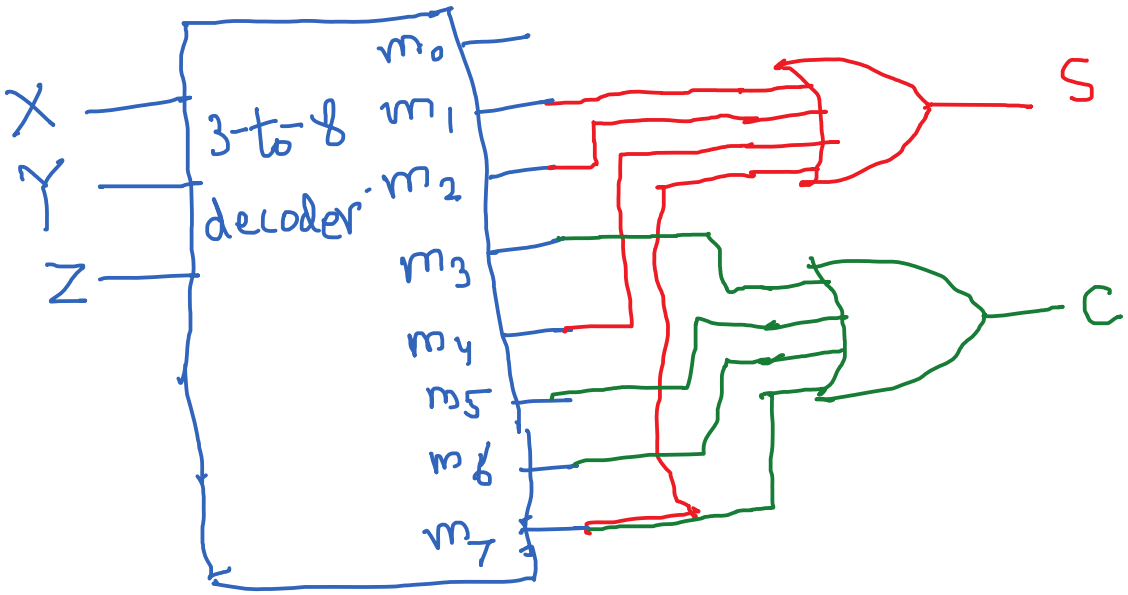
From Page 2 of Lesson 10

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Part a)

$S = m_1 + m_2 + m_4 + m_7$

$C = m_3 + m_5 + m_6 + m_7$



1) continued

Part b)

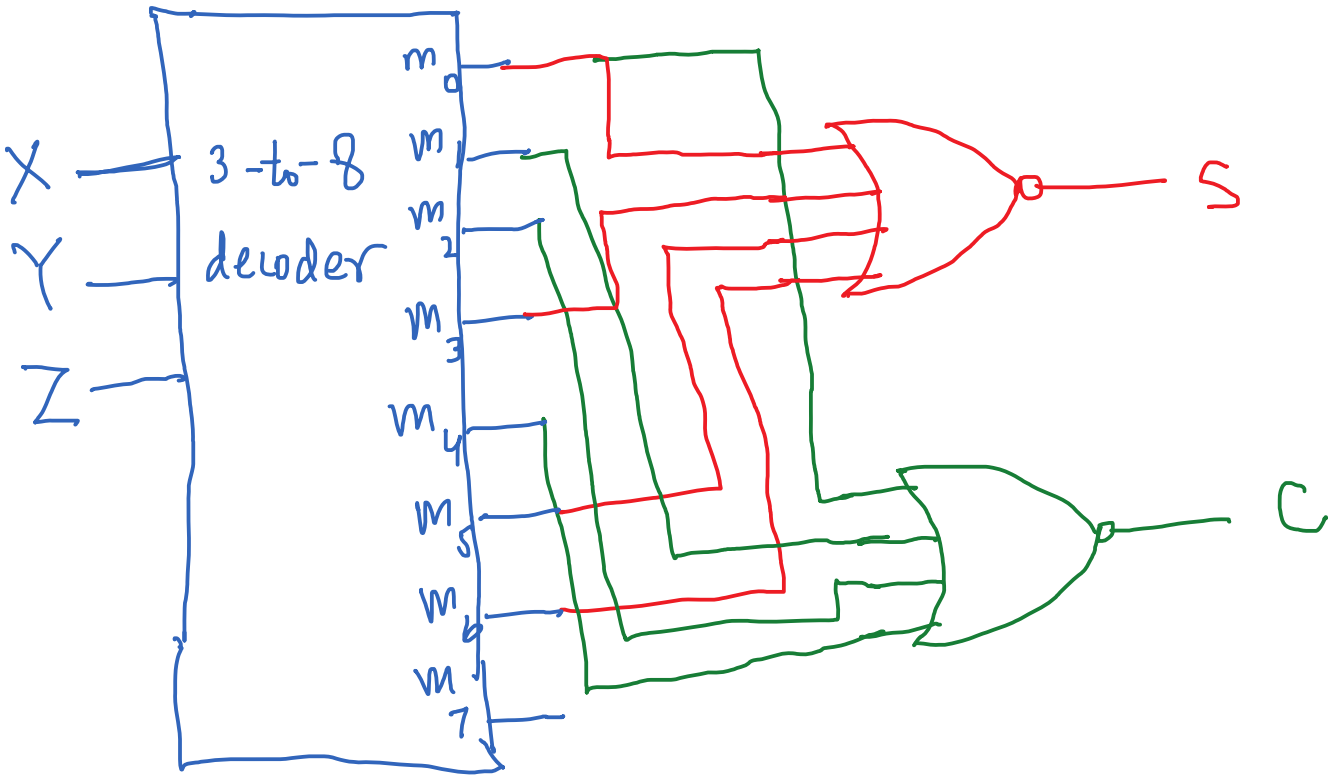
$$S = M_0 M_3 M_5 M_6 \qquad \overline{S} = \overline{M}_0 + \overline{M}_3 + \overline{M}_5 + \overline{M}_6$$

$$\overline{S} = m_0 + m_3 + m_5 + m_6$$

$$S = \overline{\overline{S}} = \overline{m_0 + m_3 + m_5 + m_6}$$

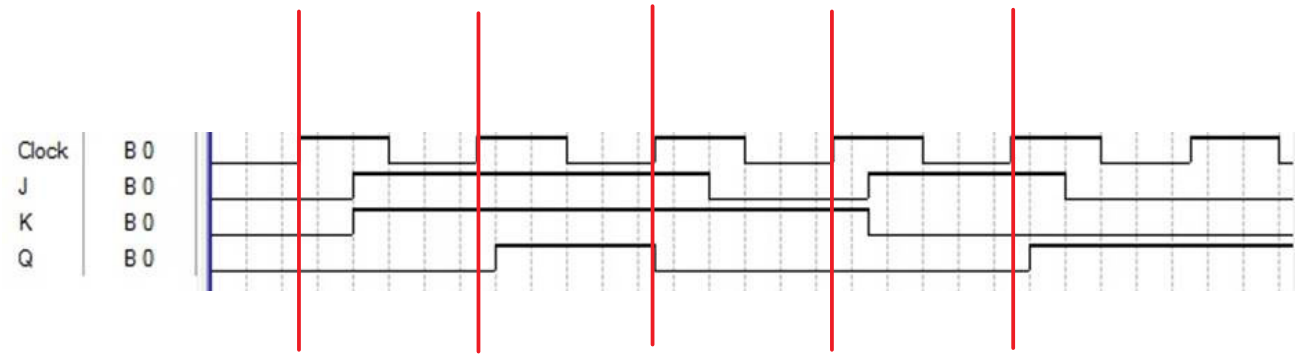
Similarly

$$C = M_0 M_1 M_2 M_4 = \overline{m_0 + m_1 + m_2 + m_4}$$



11.7) Q only changes at the Rising Edge of the clock

Rising Edge	J	K	Mode	Q
1	0	0	No Change	0
2	1	1	Toggle	1
3	1	1	Toggle	0
4	0	1	Reset	0
5	1	0	Set	1
6	0	0	No Change	1



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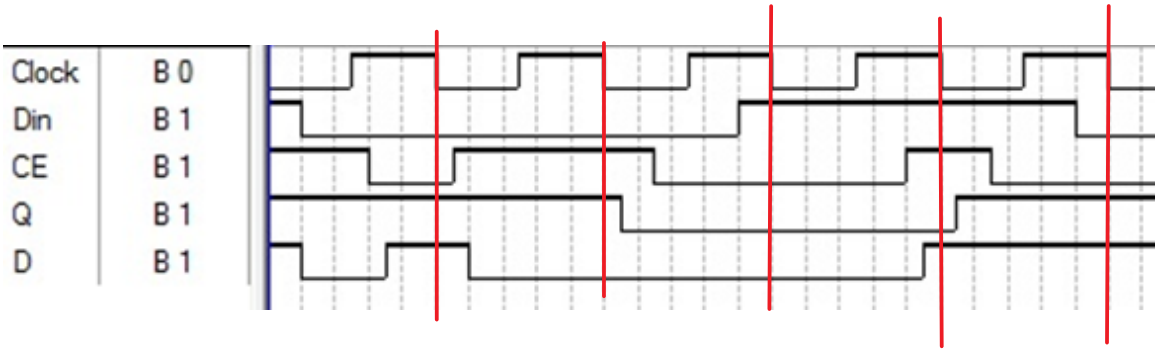
3) Problem 11.8a
Q reads in the value of Din when CE=1 and the clock is falling.



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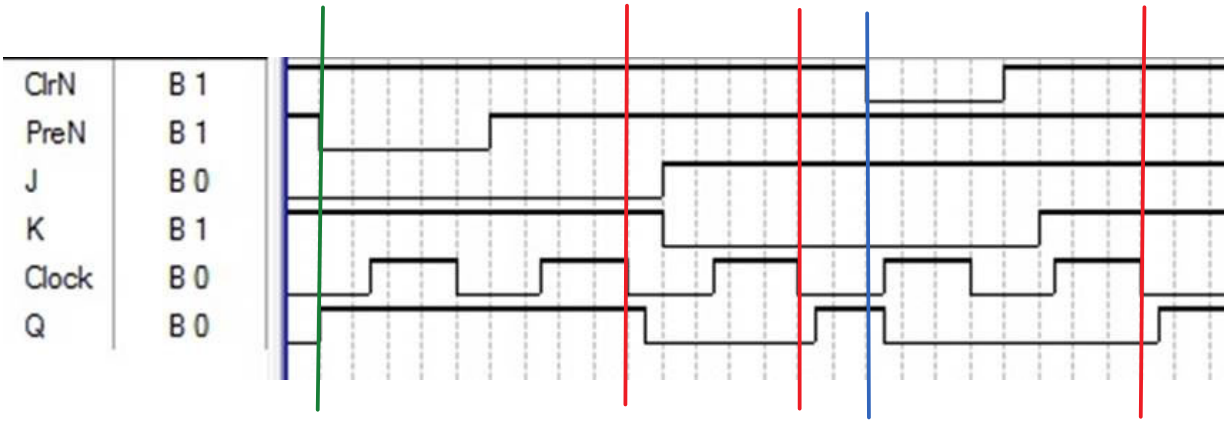
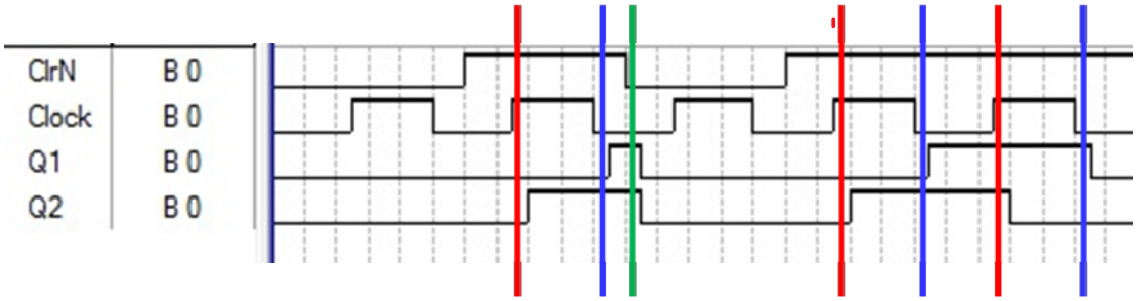
4) Problem 11.9

a) Ignore any normal inputs when an asynchronous input is active.

Event	J	K	Mode	Q
Preset Active	ignore	ignore	Set	1
2nd falling edge	0	1	Reset	0
3rd falling edge	1	0	Set	1
Reset Active	ignore	ignore	Reset	0
5th falling edge	1	1	Toggle	1



b) Q1 toggles on the **falling edge**. Q2 toggles on the **rising edge**. Both are cleared while ClrN is **active**.



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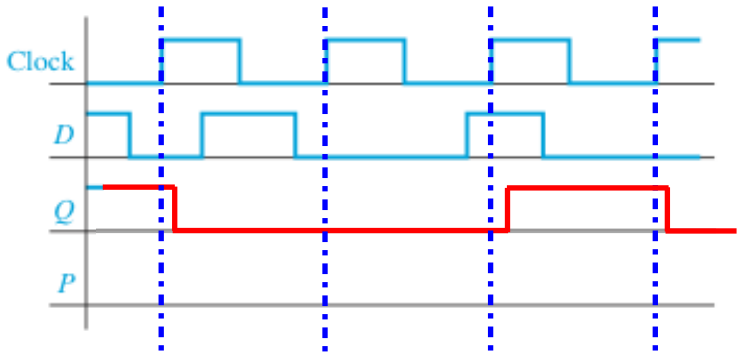
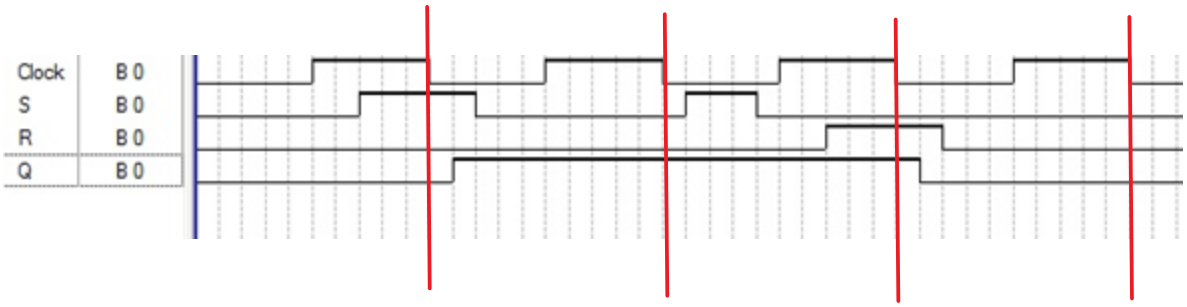
5) Problem 11.19a

11.19 Complete the following diagrams for the rising-edge-triggered D flip-flop of Figure 11-19. Assume Q begins at 1.
(a) First draw Q based on your understanding of the behavior of a D flip-flop.



The problem numbers are from your text book (both the 6th and 7th edition will work)

6) Problem 11.21



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7) Problem 11.24 Notice the large delay between the clock and the change in Q_2. This is due to clock gating. If it can be helped, you should never put anything on the clock line other than the clock.